Enhanced Control for Local Helicity Injection on the Pegasus ST

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PEGASUS
Toroidal Experiment

Layout Slide (Include for Posters)

12:1 scale Panel size: 8’ x 4’

US Legal
8.5 x 14”

US Letter
8.5 x 11”

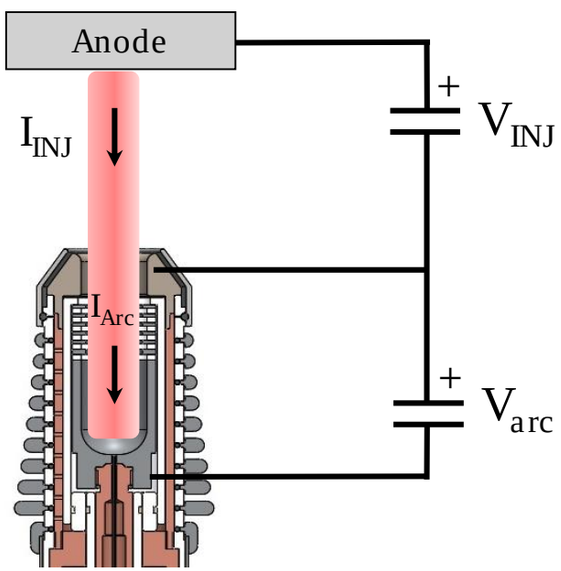
Enhanced Control for Local Helicity Injection on the Pegasus ST

Background	Hardware	Splitter Combiner	Code Testing	Future Work
Pegasus/LHI Overview	What’s an FPGA?	S/C Overview	Overview of FPGA Application Testing	Near-Term Work
Power Supply Overview	NI FPGA System Architecture	FPGA S/C Block Diagram	FPGA Noise Immunity Testing	Possible Near-Term Physics Studies
Present Control Systems Limitations	Hardware on Pegasus	I/O Requirements	Bridge Level Protection Logic Validated	Future Power System Control
FPGA Upgrade	Near-Term FPGA Implementation	State Filtering & State Diagram	FPGA S/C BenchTesting	Future FPGA Enabled Physics Studies

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Local Helicity Injection (LHI) Provides Robust Non-Solenoidal Startup on the PEGASUS ST

Plasma Parameters		Injector Parameters	
I_p	≤ 0.23 MA	$\sum I_{inj}$	≤ 14 kA
τ_{shot}	≤ 0.025 s	I_{inj}	≤ 4 kA
B_T	0.15 T	V_{inj}	≤ 2.5 kV
A	1.15–1.3	N_{inj}	≤ 4
R	0.2–0.45 m	A_{inj}	$= 2\text{-}4$ cm^2
a	≤ 0.4 m	I_{arc}	≤ 4 kA
κ	1.4–3.7	V_{arc}	≤ 0.5 kV



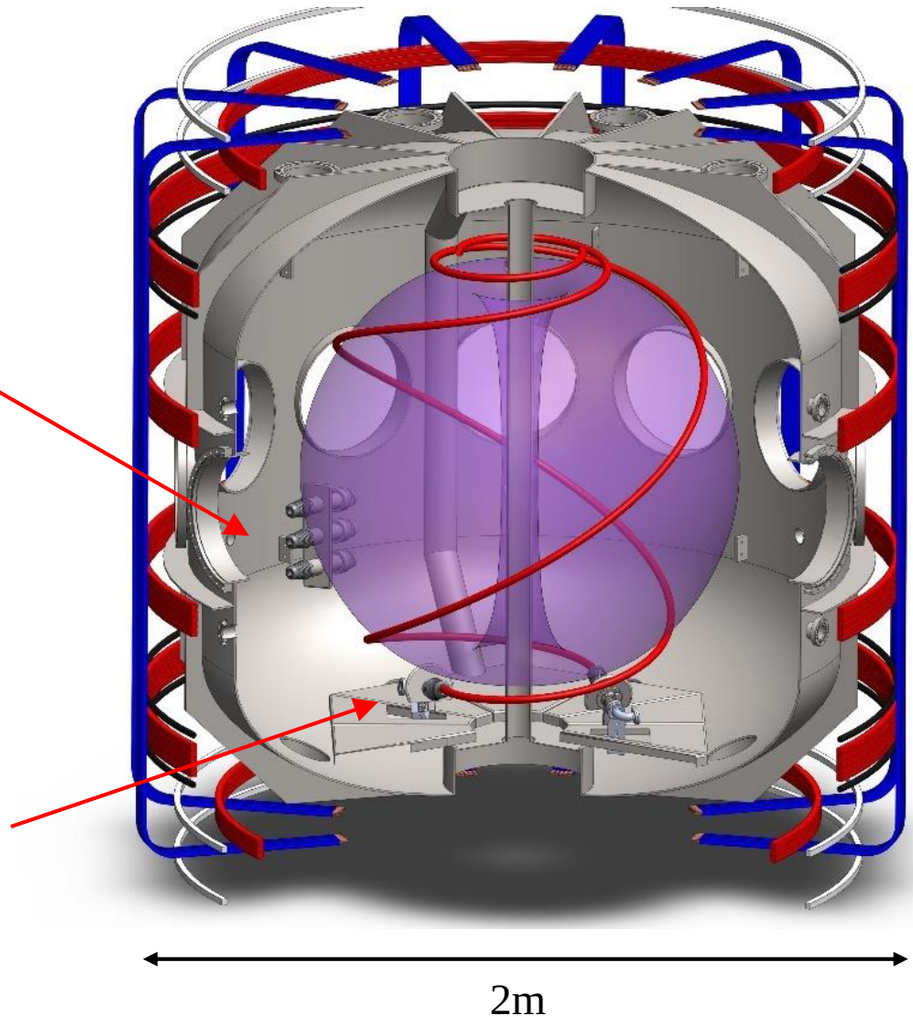
Helicity Injectors



LFS System

HFS System



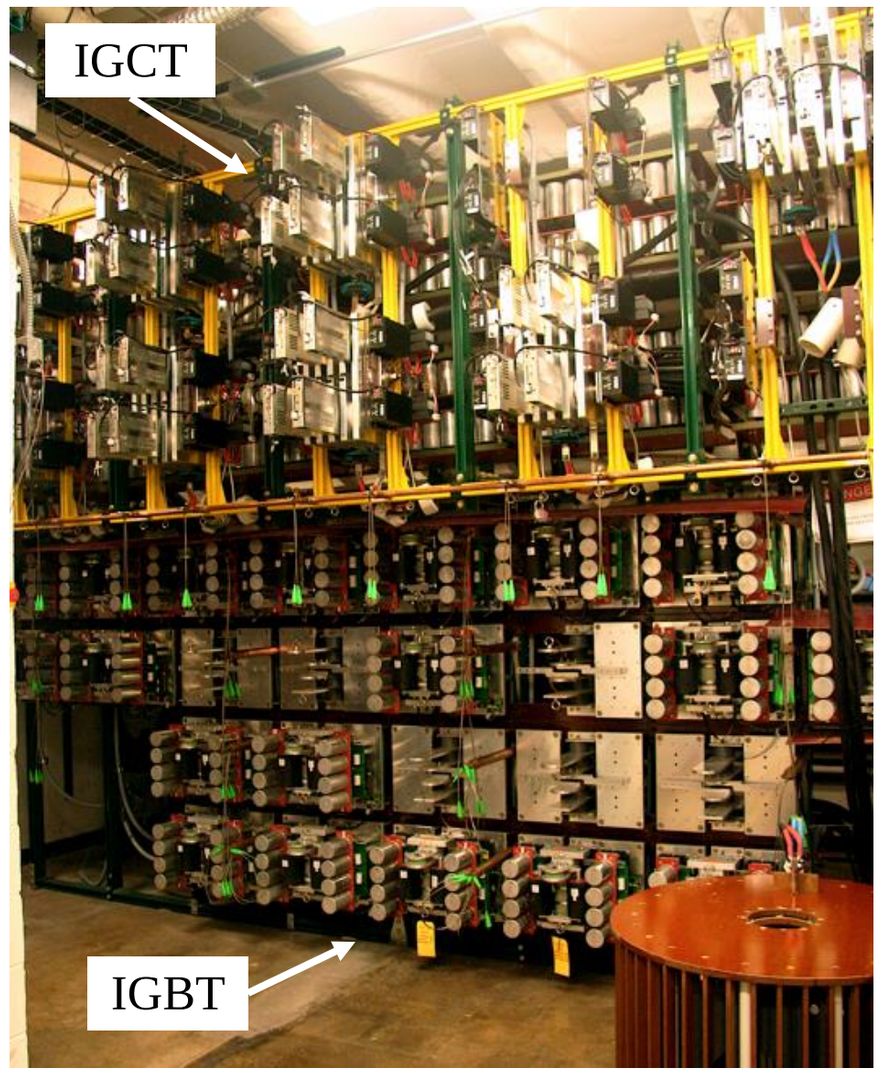


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Pegasus Driven by ~ 250 MVA Modular Power System

- Drive wide range of loads
- 35 optically isolated H-Bridges
  - 12 IGCT
  - 23 IGBT
- Analog feedback control
- Control signals multiplexed to N bridges
  - 'Splitter-Combiner' (S/C)

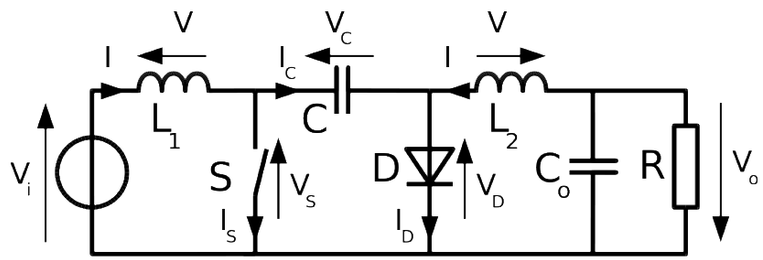
Load Types	Operating Voltage	I_{max} [kA]	Controlled Power [MVA]
Toroidal Field (TF)	900	24	21.6
Poloidal Field (PF) (x3)	900	16	14.4
Radial Coil	900	4	3.6
Divertor Coil	900	4	3.6
Ohmic Solenoid	2200	32	70.4
Injector Arc (x4)	900	4	3.6
Injector Bias (x2)	2200	12	26.4



Next Generation LHI Enabled by Planned Power Supply and Control System Upgrades

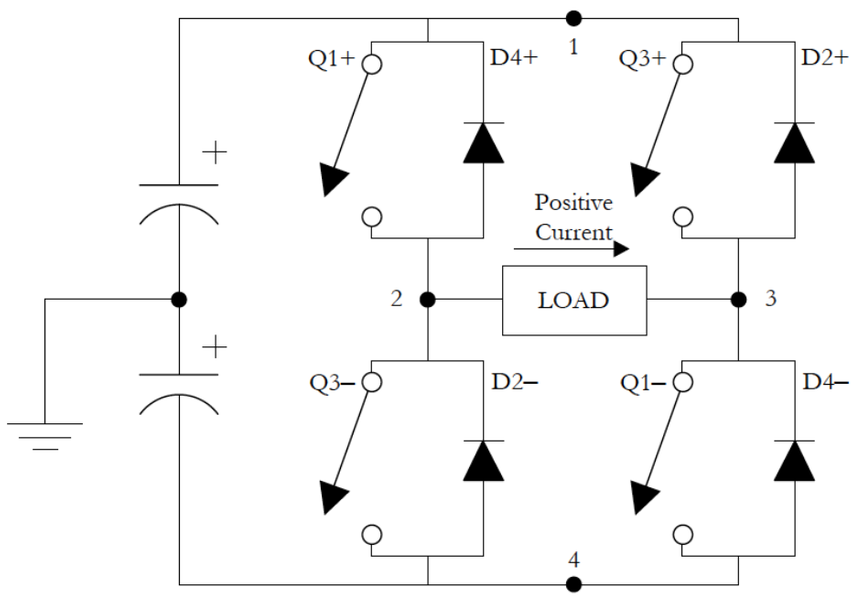
- FPGA 'Splitter-Combiner'
  - Expands number of simultaneously controllable bridges
  - Improve IGCT Protections
- Ćuk Converter Power Supply for Injector Arc & Bias
  - Low ripple programmable voltage control
- FPGA Digital Feedback Controllers
  - Programmable coil set and helicity injection control
- Increase TF (H-Bridge)
  - Increased Taylor Limit, confinement studies
- Expand PF (H-Bridge)
  - Improved position and shaping control

Ćuk Converter (Planned)



https://en.wikipedia.org/wiki/%C4%86uk_converter

H-Bridge Topology (1 of 35)



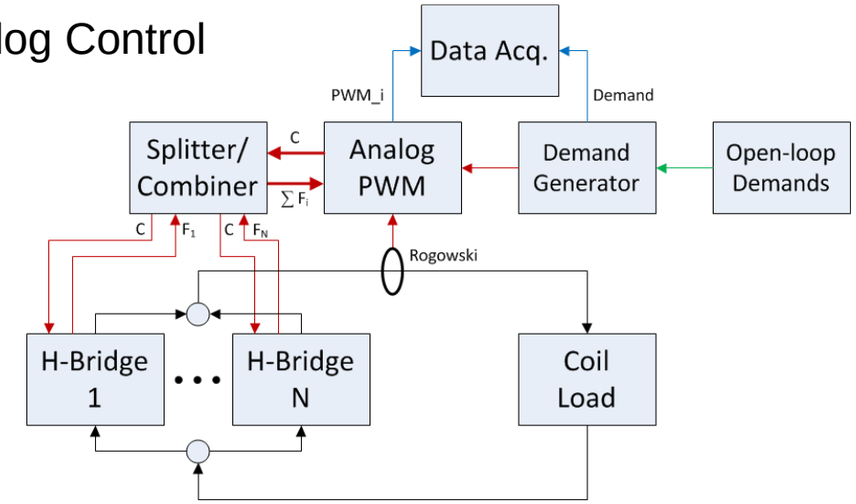
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FPGA Digital Splitter-Combiner (S/C) and Feedback Controller Expand Pegasus Control Capabilities

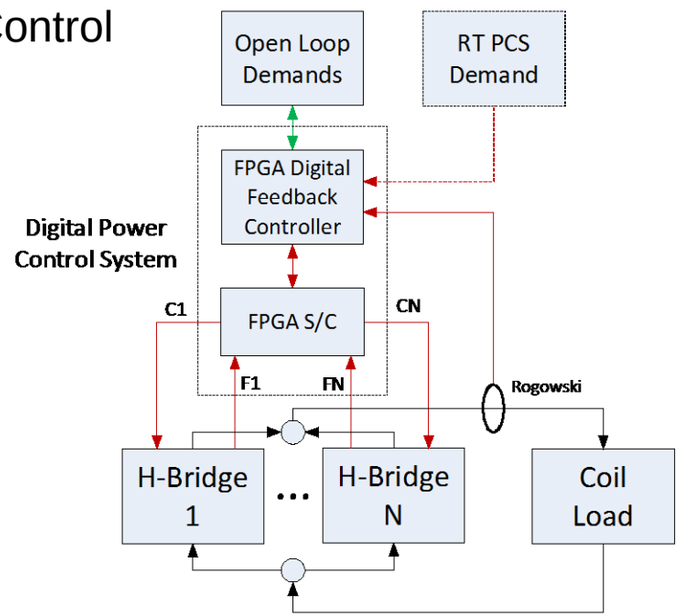
- Benefits of FPGA:
  - Programmable control algorithms
  - Expandable with off-the-shelf hardware
  - Improved EMI resilience
  - Increased stability (e.g. no comparator drift)

- S/C Improvements:
  - Additional device-level protections
  - Reduced fault response time
  - Continuous fault monitoring

Present Analog Control



Planned FPGA Control

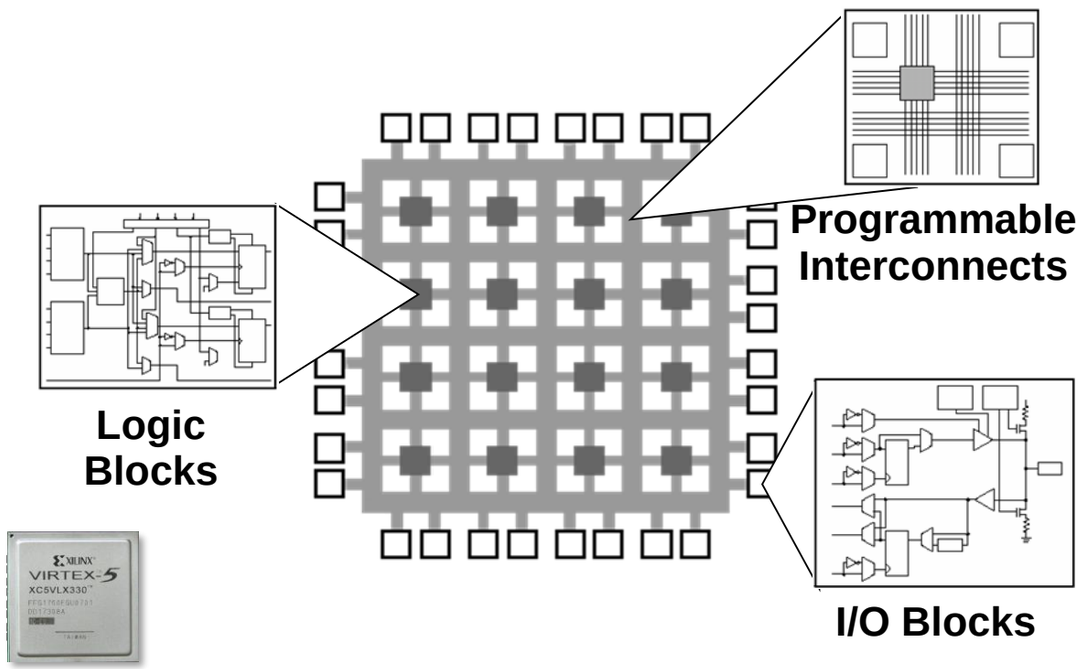


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Field Programmable Gate Array (FPGA) Technology Overview

- "Programmable hardware" via low-level logic descriptor languages (VHDL) or high-level (LabVIEW FPGA)
- Input / output interfaces
  - Analog and Digital I/O
- Clocks / timers
  - 10, 40 MHz fundamental
- Direct Memory Access (DMA) interfaces
  - FPGA↔Realtime PC data exchange
- PCI, PXI bus interfaces
  - Inter-FPGA signaling, data exchange, timing

FPGA Resource Types

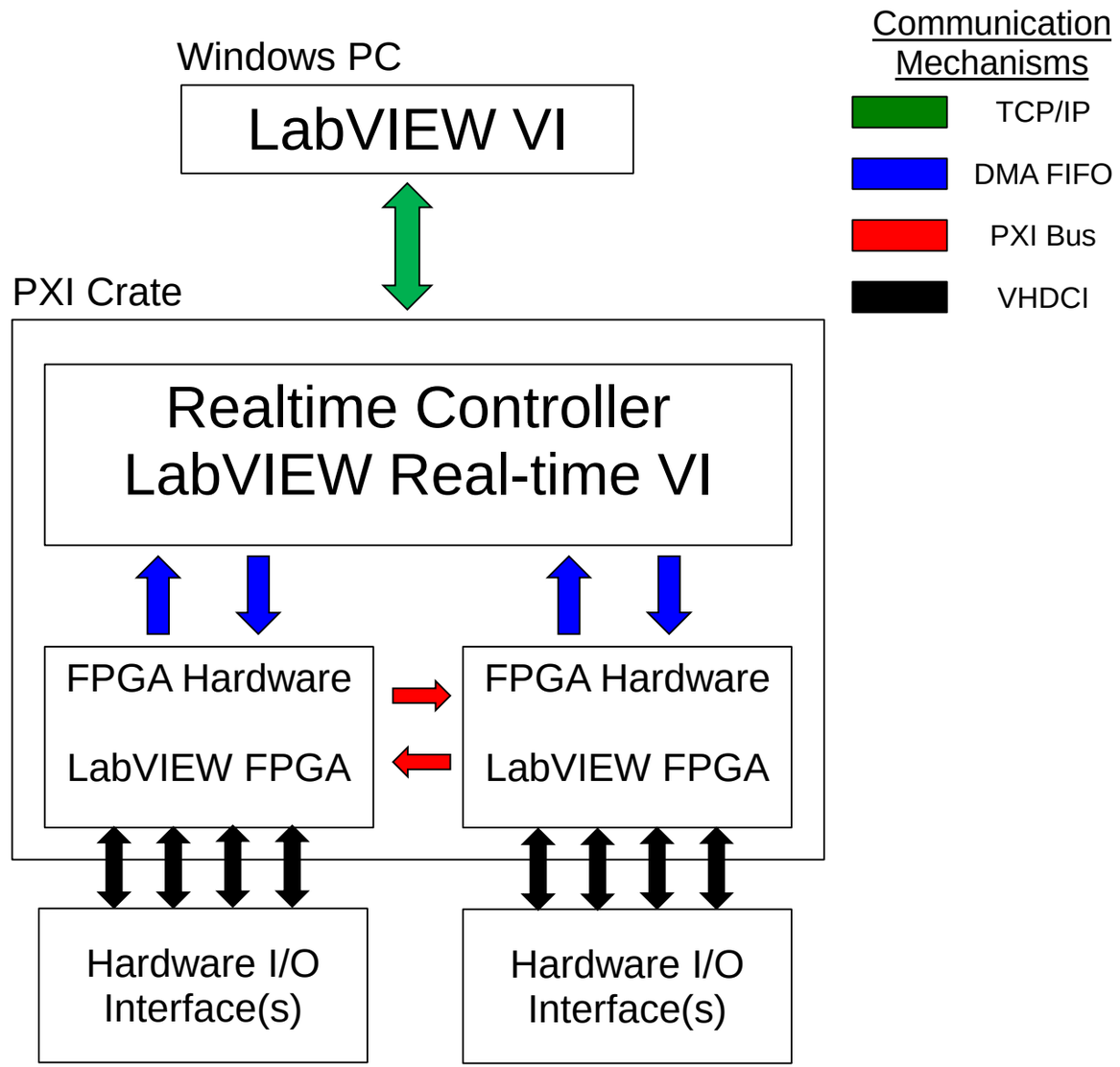


Source: NI.com, Introduction to LabView Real-Time and FPGA

https://forums.ni.com/t5/Community-Documents/Introduction-to-LabVIEW-Real-Time-and-FPGA-Presentation-and/ta-p/3515914

National Instruments Labview FPGA Platform Provides Flexible Control System Architecture

- Software Hierarchy
  - LabVIEW
    - General-purpose language, no timing guarantees
  - LabVIEW Real-time
    - ~100s kHz – class timing guarantees
    - Can act as data processor and pass-through for FPGAs
  - LabVIEW FPGA bit file
- Hardware Hierarchy
  - Windows PC
  - Real-time PXI controller
    - Real-time OS, embedded hardware control interfaces
  - FPGA Modules
  - Plant I/O Interface
- Applications can have varying levels of complexity
  - FPGA only
  - Multiple FPGAs (and PXI intra-FPGA signaling)
  - FPGA(s) + RT host
  - FPGA(s) + RT host(s) + Windows host



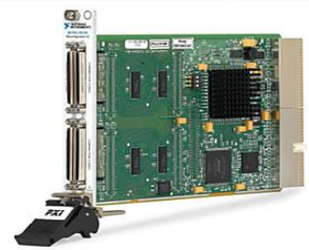
FPGA Hardware Employed for Pegasus System

- NI PXI 7852R “Hybrid” FPGA (x2)
  - 8 AI, 8 AO
  - 96 DIO
- NI PXI 7813R “Digital” FPGA (x1)
  - 160 DIO channels
- PXIe-1062Q Crate (x2)
  - Houses embedded controller (PXIe-8133 / PXIe-8135) and FPGA units
  - Real-time LabVIEW control capability
  - TCP/IP remote control capability
- Electro Standards Laboratory (ESL) Custom TTL↔Optical Transceiver (x7)
  - Convert 20 TTL I/O pairs to 20 Optical TX/RX pairs
  - Optical signaling compatible with IGBTs & IGCTs

NI 7852R Hybrid FPGA



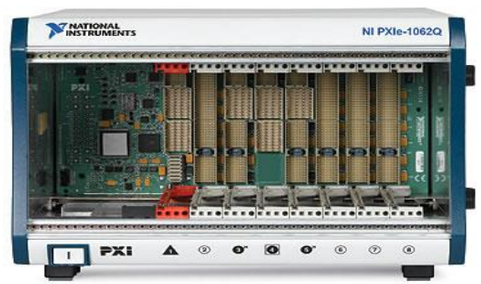
NI 7813R Digital FPGA



NI 8133 PXIe Controller



NI PXIe-1062Q Crate



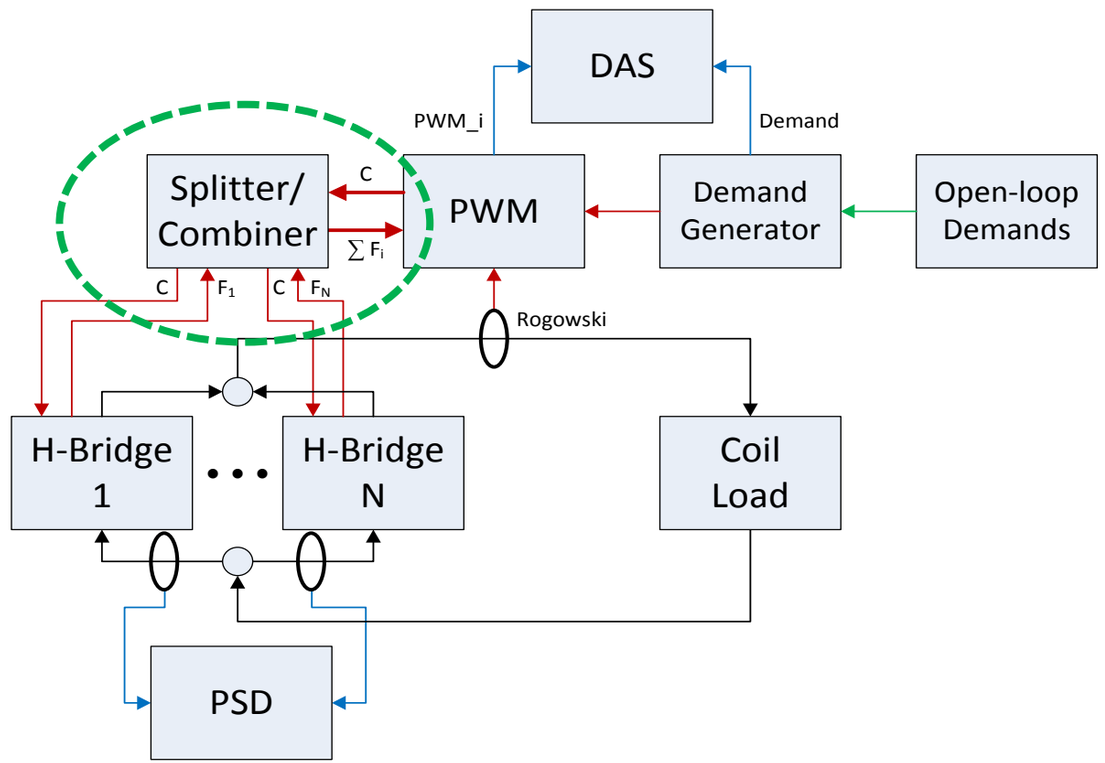
ESL TTL↔Fiber Transceiver (front and back connectors)



FPGA Splitter-Combiner Chosen as First Application

- Addresses technical requirements for many applications:
  - Fundamental for planned upgrades
- Improvements enabled by FPGA S/C:
  - Continuous fault monitoring
  - Improved fault response time
  - More robust device protection
  - Increased number of controllable bridges

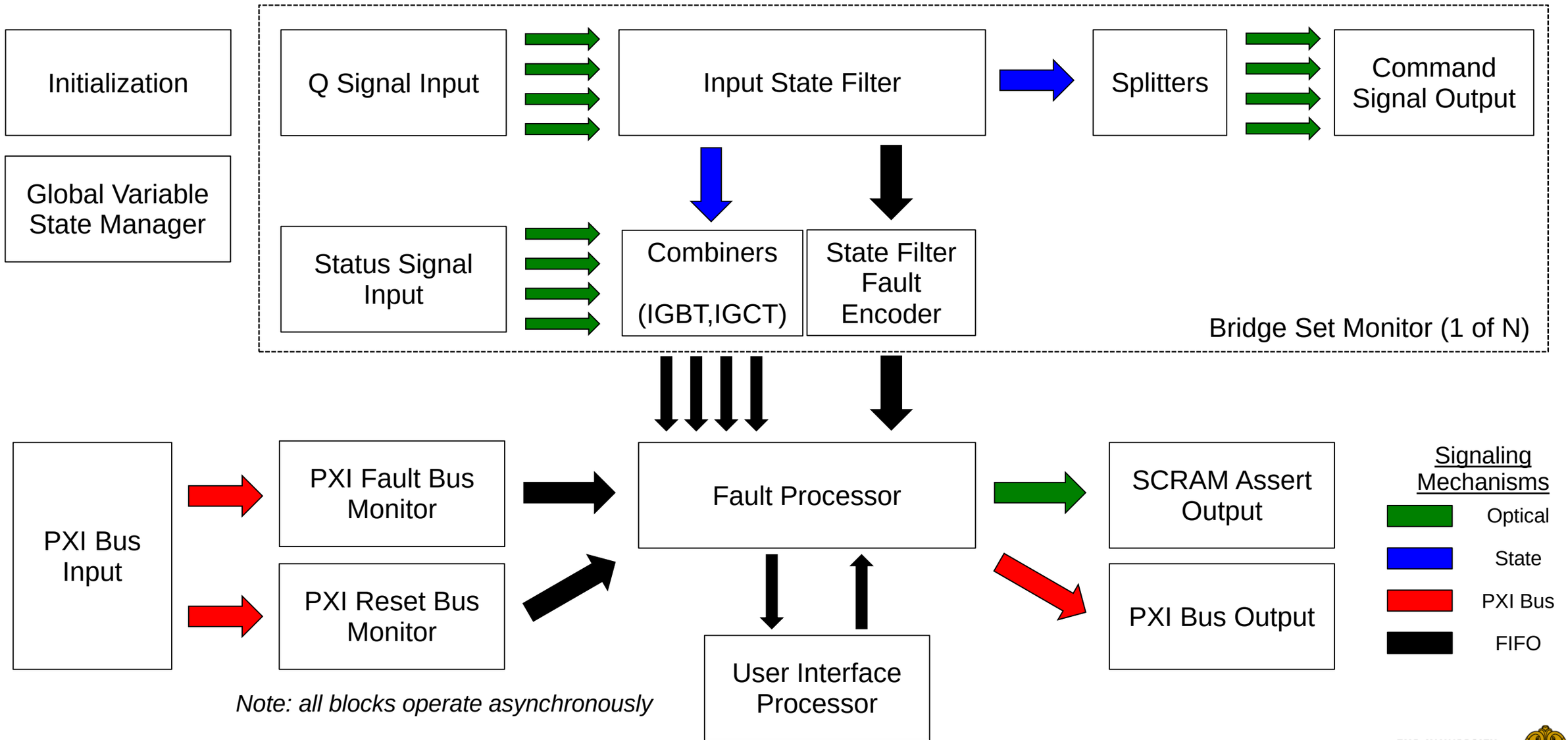
S/C Block Replacement



FPGA Splitter/Combiner Improves Device-Level Protections

- Splitter Functionality Retained:
  - Multiplexing of command signals to N bridges
- Combiner Functionality Retained:
  - Device-level interpretation of IGBT/IGCT status signal
  - Aggregation of bridge status signals to single assertion of “Coil Set OK”
  - Fault assertion for SCRAM system
  - Identification of faulted device
- FPGA Enabled Improvements:
  - Continuous monitoring of device status
  - Protection from invalid PWM commands (state filter)
  - Improved fault response time (25-100 ns)

FPGA Splitter-Combiner Block Diagram



Note: all blocks operate asynchronously

Input/Output Requirements Satisfied by Multi-FPGA System

Present Power Supply Configuration

Load	Typ. V	I_{max} [kA]	# of Bridges	Bridge Type	Power S [MVA]
TF	900	24	6	2Q	21.6
PF 23	900	16	4	2Q	14.4
PF 67	900	16	4	2Q	14.4
PF 45	900	8	2	4Q	7.2
Radial Coil	900	4	1	2Q	3.6
Divertor Coil	900	4	1	2Q	3.6
Ohmic Solenoid	2200	32	8	4Q	70.4
Injector Arc	900	4	1	4Q	3.6
Injector Bias	2200	12	3	1Q	26.4

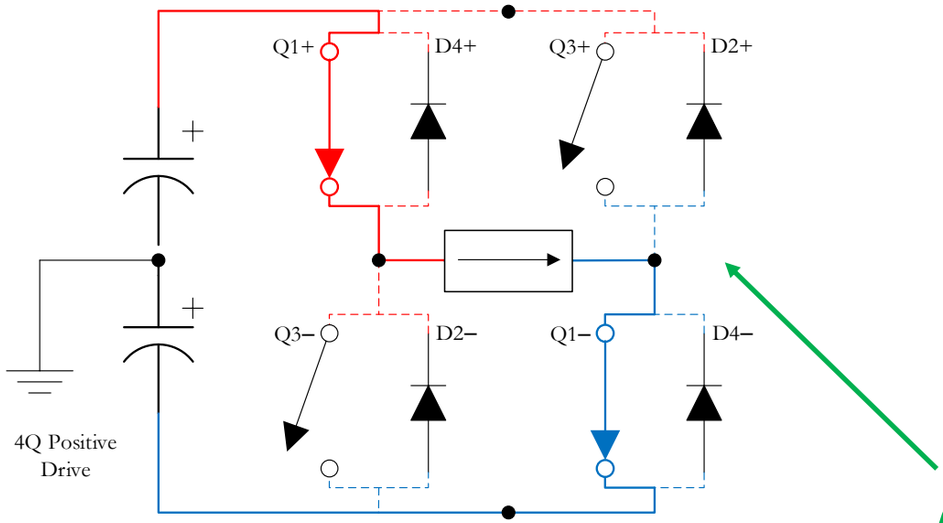
- 3 FPGAs meet I/O needs
- Intra-FPGA communicates via fast PXI bus

	Optical In	Optical Out	DIO
Status IN	93	-	93
PWM Commands	27	-	27
Command OUT	-	93	93
Aggregate Fault	-	11	11
SCRAM		1	1
TOTAL	**120**	**105**	**225**
AVAILABLE	160	160	320

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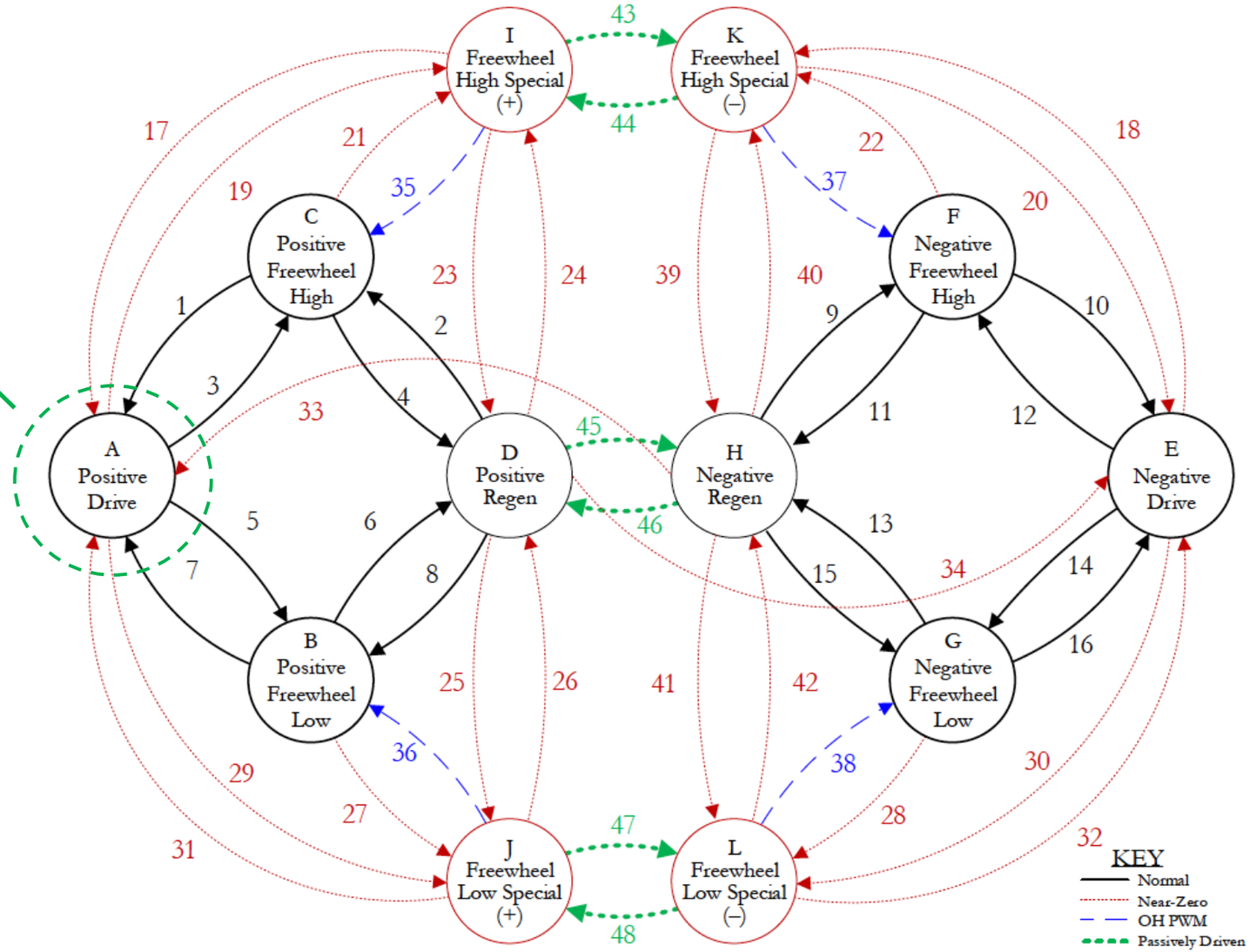
FPGA Enabled State Filtering Increases Device-Level Protections

Configuration of 4Q Bridge in State A



- State navigation controlled by PWM
- S/C filters PWM commands; only valid commands sent to bridges
- Enforces minimum dwell times during operation & fault handling

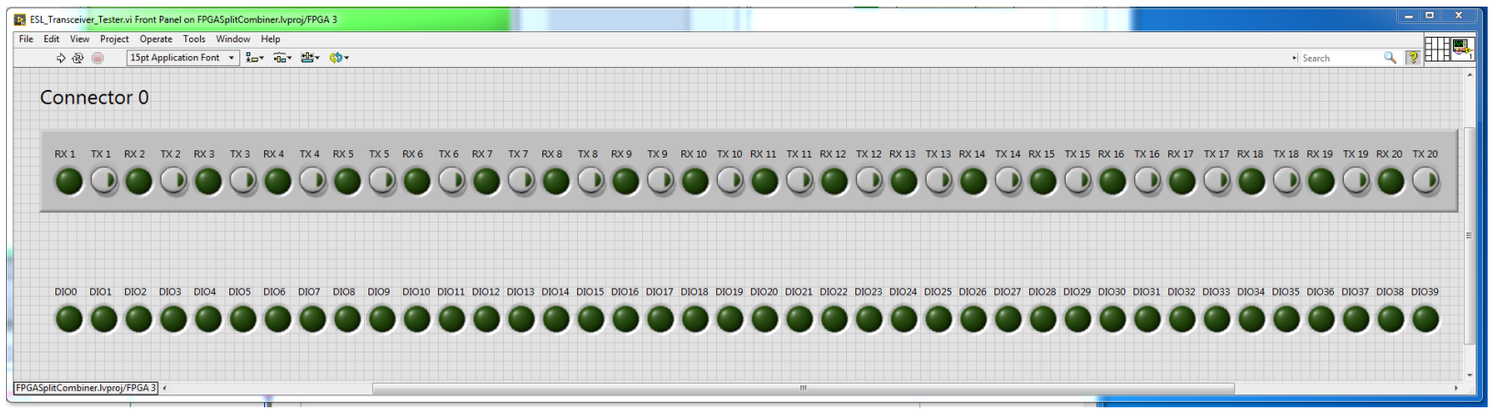
4 Quadrant Bridge State Diagram



C. Pierren, APS-DPP, 2017

Functionality of Custom Electro Standards Laboratory (ESL) Transceivers Verified

Pinout Verification VI: TX State Toggled by User



Seven ESL 6760 Units Under Test



- Critical for optical interfacing
- FPGA used to verify ESL Transceiver
  - Test waveforms, clock / pulse generators, etc.
  - 23 VIs developed for transceiver interfacing
  - Interface library also applied to S/C
- Result: Pegasus requirements satisfied

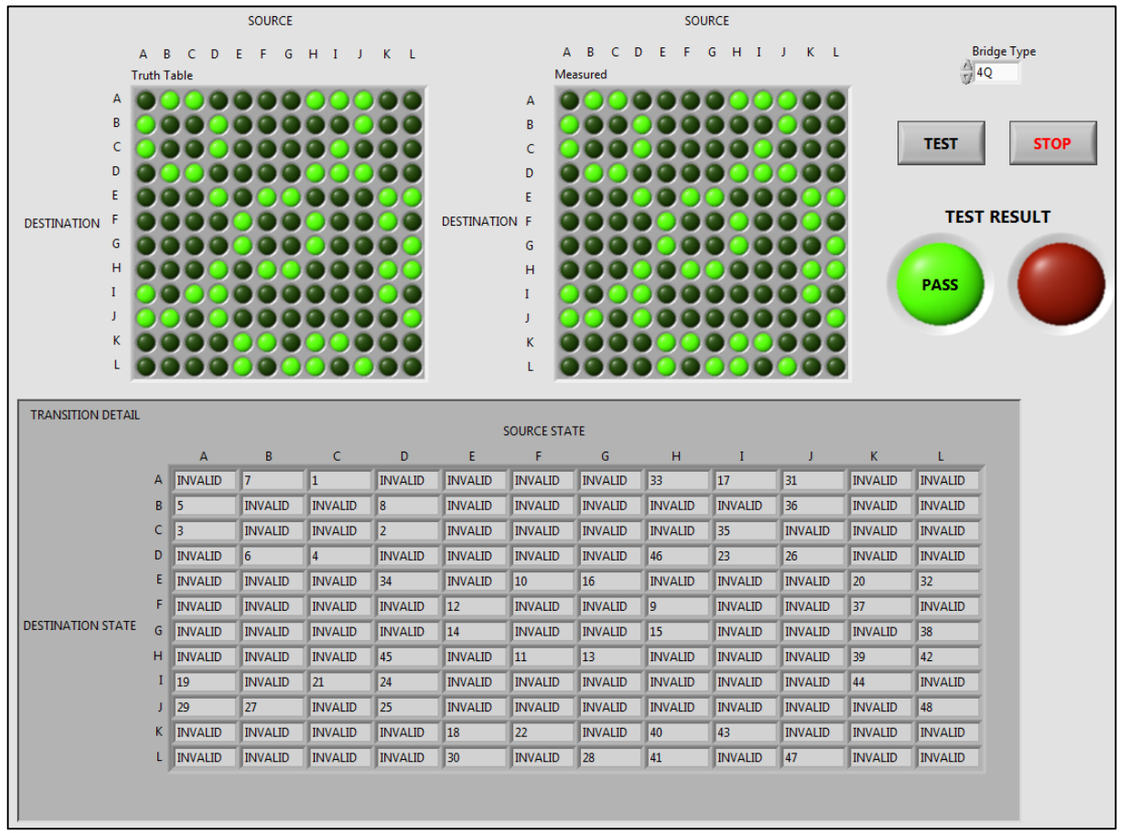
Spec Verified	Description
Physical I/O Mapping	TTL ↔ Optical TX/RX
Optical Power	Signal above threshold
Bandwidth	Verify data bit rate 10Mbps
Crosstalk	Quantify susceptibility (none)
Noise susceptibility	Test EMI resilience (robust)

Noise Immunity Testing Indicates Optical Interface Improves EMI Resilience

- FPGA system deployed in same environment as present control system
  - Monitored for noise induced state changes every 25 ns
- Tested during operational period with uncharacteristically high levels of noise
  - Present system experienced 4 faults that halted operations
  - FPGA system did not fault: robust to this environment
- Noise resilience should improve reliability and increase run time

State Detection and Transition Filter Logic Verified with Custom Labview FPGA Test Platform

- Core logic implemented:
  - Detect current state of H-bridge
  - Filter states; only valid states, transitions sent to bridges
- Tested with external test platform:
  - Challenged all possible states
  - Challenged all possible state transitions
  - Recorded inferred states and transition validities
  - Compared to design specifications
- Implementation passed hardware proof



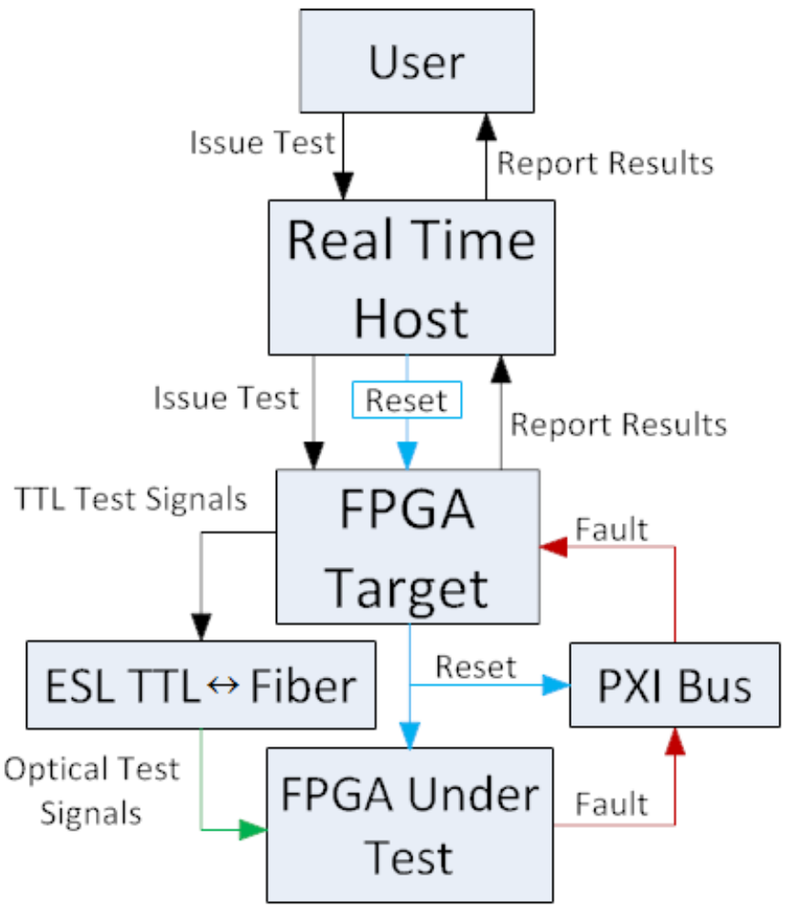
FPGA S/C Functionality to be Verified by Full System Testing Platform Before Deployment

- Created test platform to source arbitrary optical signals:
  - FPGA Target generates user programmed ‘PWM’ and ‘Status’ signals for FPGA Under Test
  - Real Time Host interfaces between User and FPGA Target
  - Target monitors PXI Bus for challenge induced faults
  - Challenge results reported to user
- Mechanics of test bench verified:
  - Proof of concept test
  - Enables automation of S/C testing
- Challenge sequences to verify S/C fault response:
  - IGBT & IGCT status faults
  - Invalid state encoding
  - Invalid state transition command
  - Insufficient state dwell time

  } Fault Modes

  - Valid transit of state diagram → No fault

Test Platform



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Development & Deployment Plan for Power Supply & Control System Upgrades

Near-Term

- FPGA Splitter/Combiner
  - Expands control channels; TF upgrade
  - IGCT protection
- Ćuk converter for injector Arc and Bias supplies
  - Low ripple voltage control
- FPGA digital PWM
  - Programmable coil & LHI control
  - Advanced control algorithms

Proposed

- DNB power supply & control
- RF/EBW power supply & control
- FPGA replacement of CAMAC timing modules

Physics Studies Enabled by Planned & Proposed Upgrades

- Helicity Injection Control:
  - Helicity drive scans
  - Potential for tandem operation of low-field and high-field side helicity injection
- Increased TF:
  - Explore higher TF operating space relevant to start-up on larger machines
  - Increased Taylor limit studies
- PF Expansion:
  - Improved vertical position control
  - Better coupling to helicity injectors
- OH Operations:
  - Impurity studies
  - Taylor limit studies
  - LHI to OH handoff
- DNB Control:
  - Plasma kinetic & impurity measurements
  -
- RF/EBW Control:
  - Electron heating
  - Current drive

Summary: FPGA Technology Applied to Pegasus & Pegasus-E

- FPGAs improve control and support expansion of Pegasus power supply
  - Commercial off-the-shelf hardware and software
- FPGA S/C system designed as first application
  - Protects all power supplies and enables expansion
  - Improves fault response and monitoring
  - Improves device-level protections
- Hardware & design verification in progress prior to powered testing
- Next steps:
  - Ćuk power supplies: Injector Arc & Bias
  - FPGA Digital Control
  - DNB, RF/EBW power supply

Pegasus Power Systems



FPGA Hardware Provides Flexible Control



FPGA Splitter-Combiner Design

Hardware & Software Verification

Planned Upgrades to Control System & Power Supplies

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