Development of Fully Digital Control of Pegasus Power Systems

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PEGASUS Toroidal Experiment

Layout Slide (Include for Posters)

12:1 scale Panel size: 8’ x 4’

US Legal
8.5 x 14”

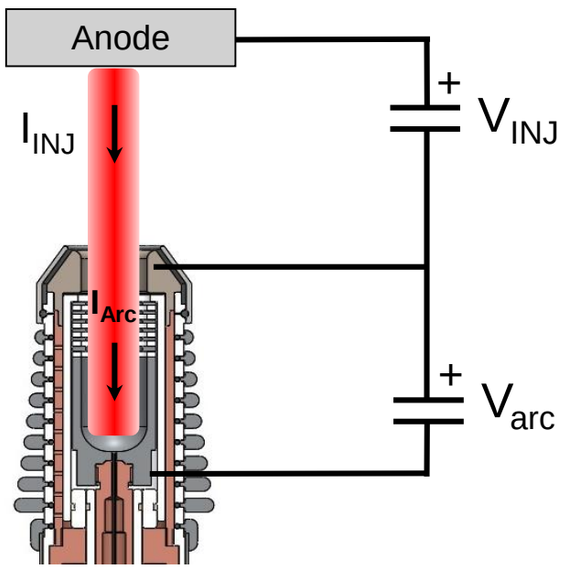
US Letter
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Development of Fully Digital Control of Pegasus Power Systems

Pegasus Overview	Physics Motivation	FPGA S/C	FPGA PWM	Future Controls / Exp.
Pegasus Overview	OH: LHI Coupling Taylor Limit VB Thomson Baseline	FPGA SC Improves Device Protections	PWM Overview	Single Cuk Module Testing Results
Power Supplies	PF Expansion: Better shape position control	FPGA SC Block Diagram	High Level Block	Modular Cuk Approach Customizable Power Supplies
Present Control	TF Expansion: LHI scaling, CHI and EBW	FPGA SC Verification & Deployment	Co-Simulation / Status I	Future Development & Deployment
Digital Control	Cuk: Vinj(t) control TF x 6 Longer pulse lengths	FPGA SC protection / results	Optical Sigma Delta	Summary Physics Enabled by Control Upgrades

Local Helicity Injection (LHI) Provides Robust Non-Solenoidal Startup on the PEGASUS ST

Plasma Parameters		Injector Parameters	
I_p	≤ 0.23 MA	$\sum I_{inj}$	≤ 14 kA
τ_{shot}	≤ 0.025 s	I_{inj}	≤ 4 kA
B_T	0.15 T	V_{inj}	≤ 2.5 kV
A	1.15–1.3	N_{inj}	≤ 4
R	0.2–0.45 m	A_{inj}	$= 2\text{-}4$ cm^2
a	≤ 0.4 m	I_{arc}	≤ 4 kA
κ	1.4–3.7	V_{arc}	≤ 0.5 kV



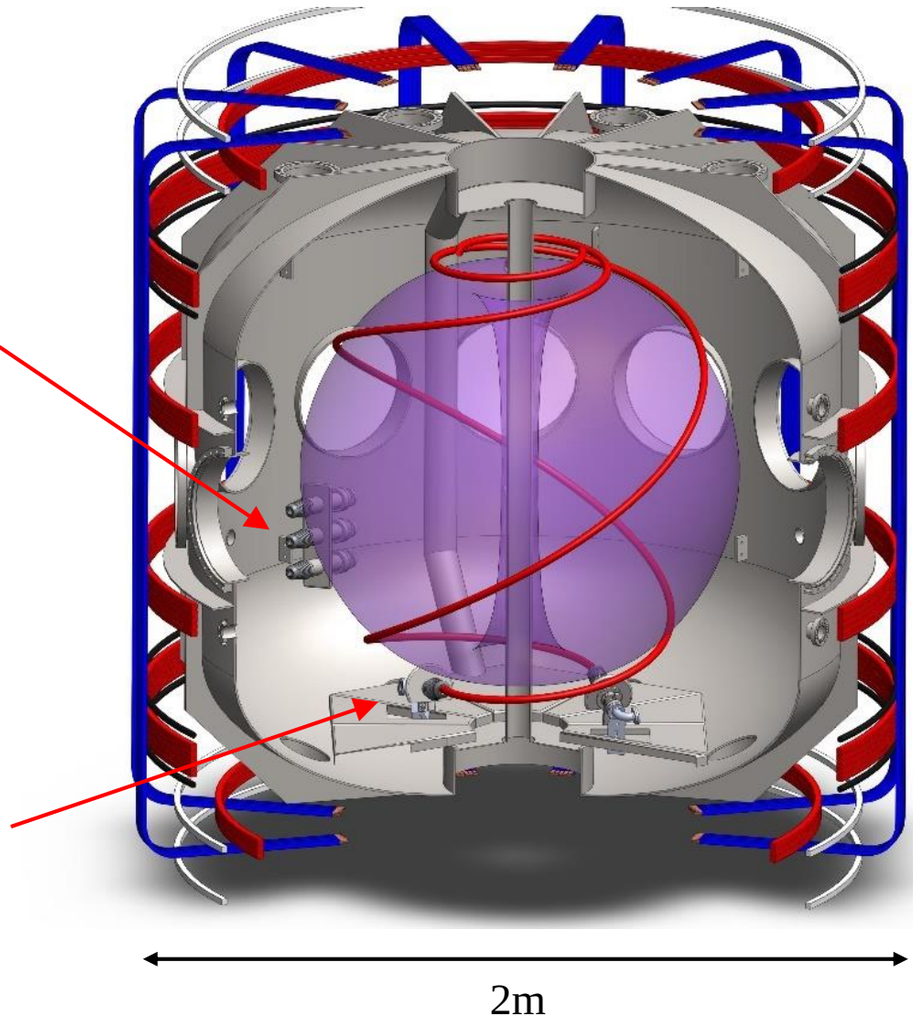
Helicity Injectors



LFS System

HFS System

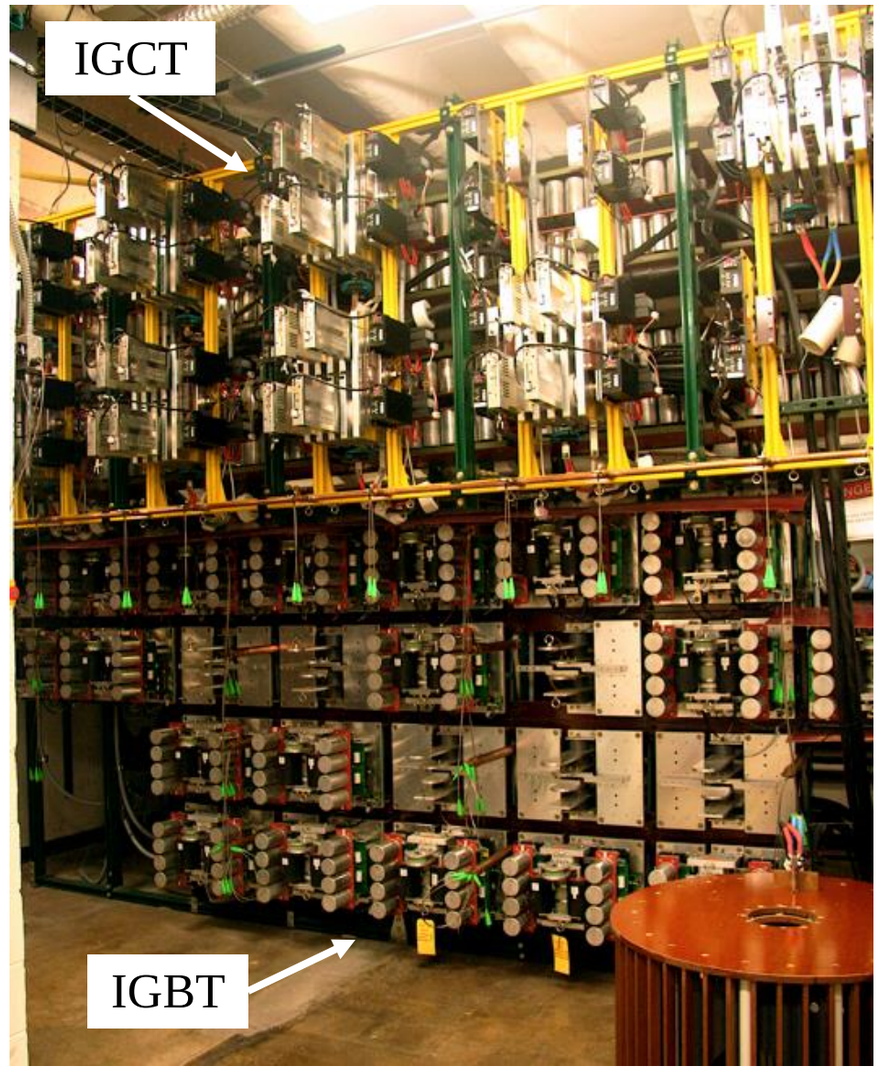




Pegasus Driven by ~ 250 MVA Modular Power System

- Drives a wide range of inductive & resistive loads
- 35 optically isolated H-Bridges
  - 12 IGCT
  - 23 IGBT
- Analog feedback control
- Control signals multiplexed to N H-Bridges
  - 'Splitter-Combiner' (S/C)

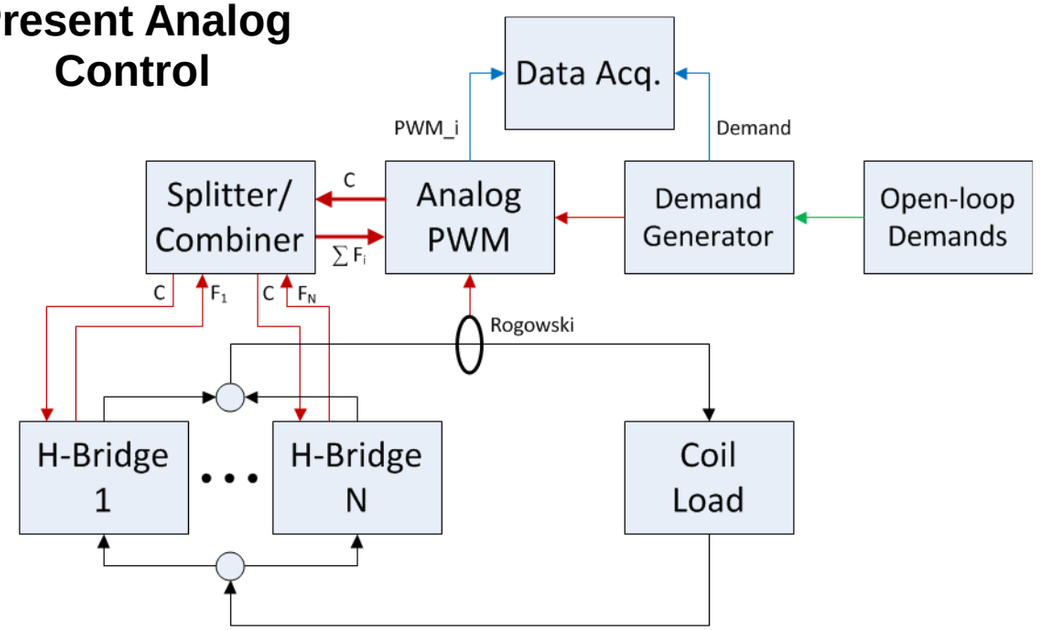
Load Types	Operating Voltage	I_{max} [kA]	Controlled Power [MVA]
Toroidal Field (TF)	900	24	21.6
Poloidal Field (PF) (x3)	900	16	14.4
Radial Coil	900	4	3.6
Divertor Coil	900	4	3.6
Ohmic Solenoid	2200	32	70.4
Injector Arc (x4)	900	4	3.6
Injector Bias (x2)	2200	12	26.4



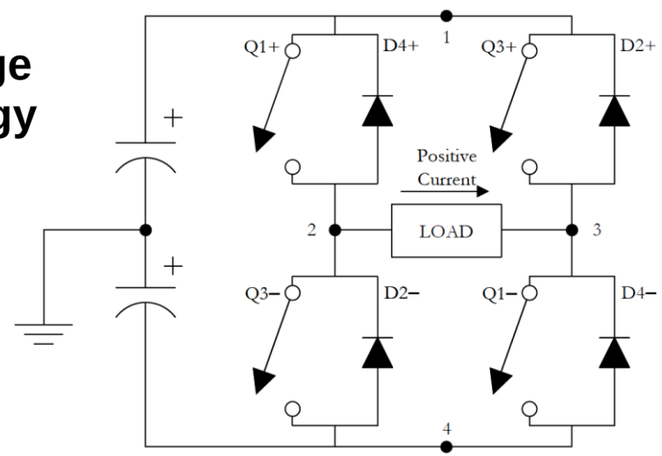
Present Analog Control Systems Not Easily Modified/Expanded

- Analog circuits susceptible to noise and comparator drift
- Analog controllers require periodic re-tuning
- Control algorithm changes require circuit modifications
- ‘Splitter’ provides no device protections
- Expansion requires building new circuits
- Ohmic (IGCT) specific protection system requires replacement

Present Analog Control



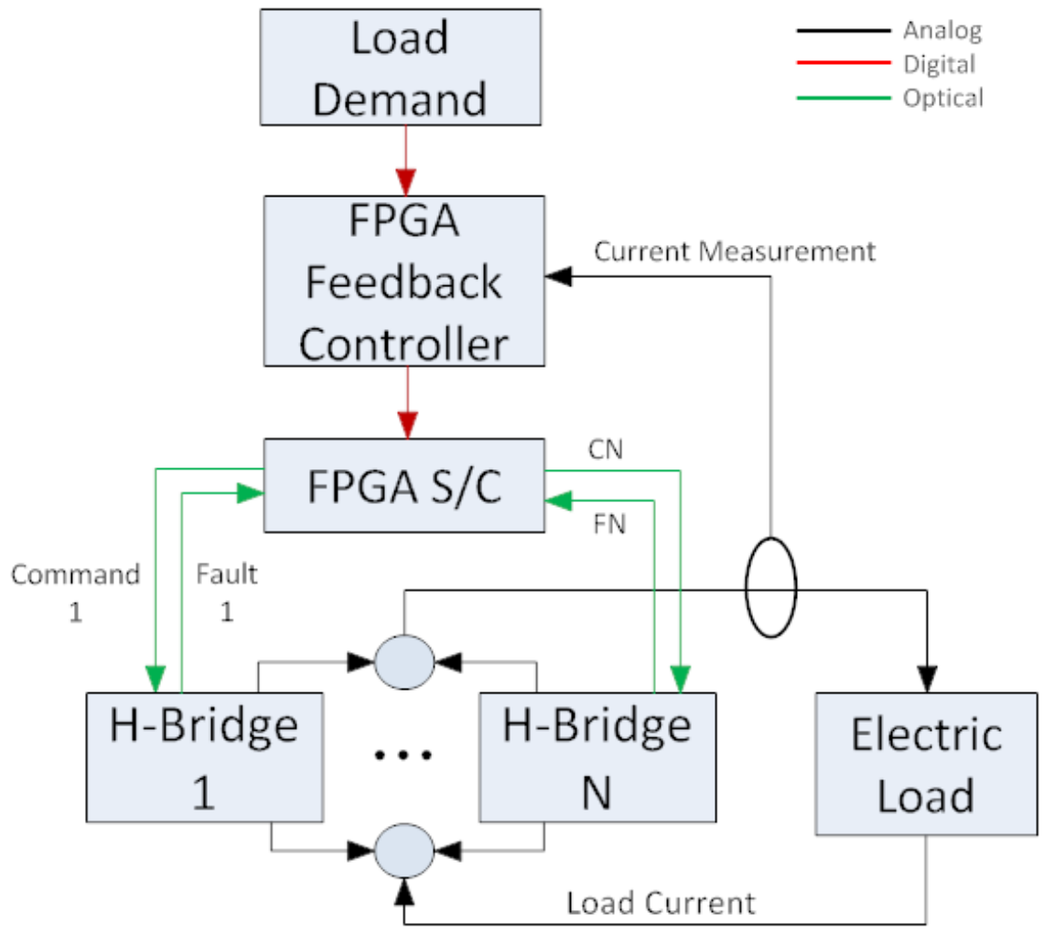
H-Bridge Topology



FPGA Digital Splitter-Combiner (S/C) and Feedback Controller Expand Pegasus Control Capabilities

- Benefits of Field Programmable Gate Array Technology (FPGA):
  - Programmable control algorithms
  - Expandable with off-the-shelf hardware
  - Improved EMI resilience
  - Increased stability (e.g. no comparator drift)
- S/C Improvements:
  - Additional device-level protections
  - Increased number of controllable H-bridges
  - Continuous fault monitoring
  - Reduced fault response time $(25 - 200\ \text{ns})$
- Regain Ohmic solenoid operations
- Expandable to future Ćuk power supplies

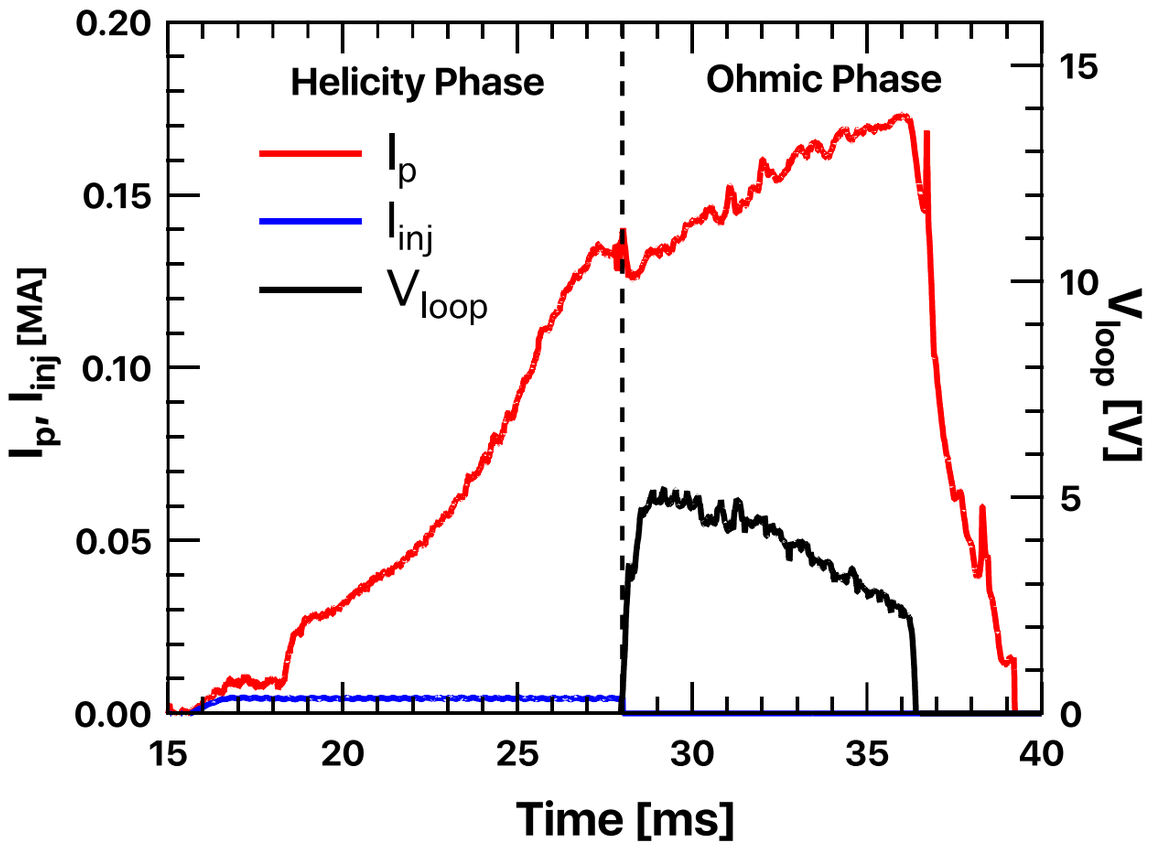
Planned FPGA Control



Improved Device-Level IGCT Protections Enables Resumed Ohmic (OH) Operation

- OH solenoid as a diagnostic tool:
  - LHI coupling to subsequent current drive
  - Taylor limit studies
    - *J.D. Weberski TP11.00112*
- OH plasma diagnostic baselines:
  - Visual Bremsstrahlung
    - *C. Rodriguez TP11.00110*
  - Thomson Scattering
  - Magnetics (MHD)
    - *N. J. Richner TP11.00111*
    - *C. E. Schaefer TP11.00113*

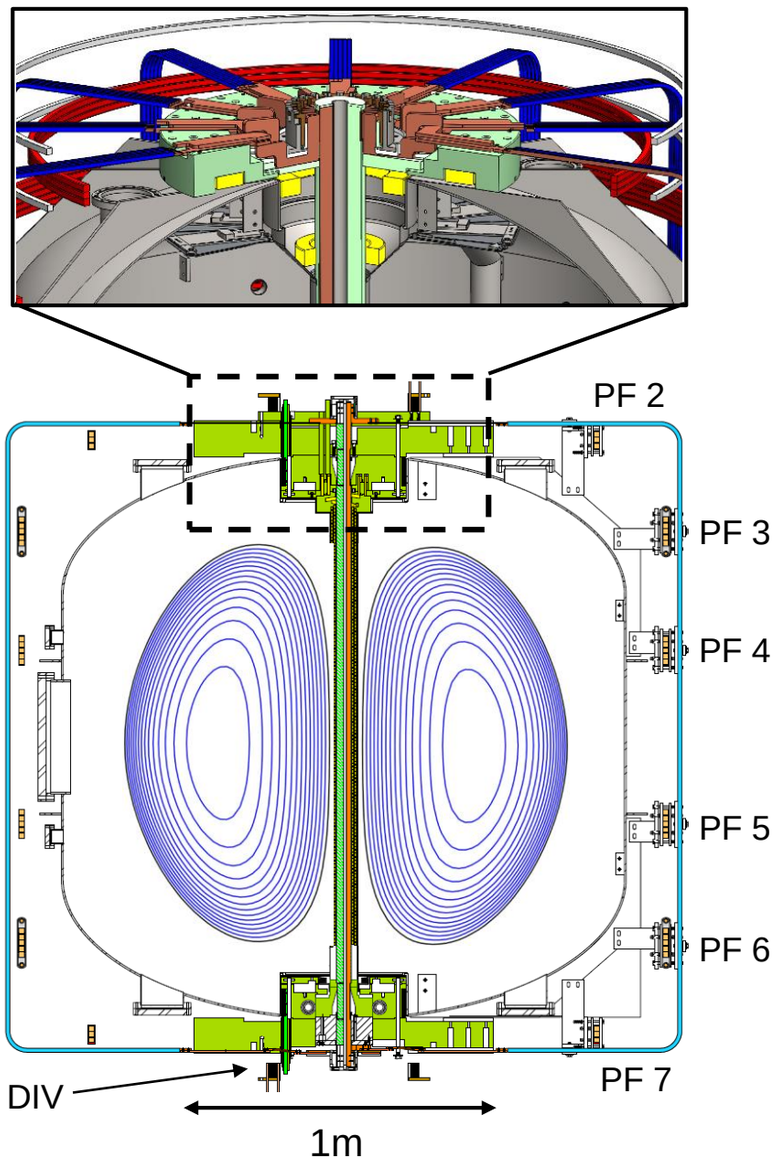
Previous LHI-to-OH Handoff



K. E. Thome, H-Mode Access and Characteristics at Near-Unity Aspect Ratio on the Pegasus Toroidal Experiment, PhD Thesis 2015

An Expanded Poloidal Field Array will Improve Shape & Position Control

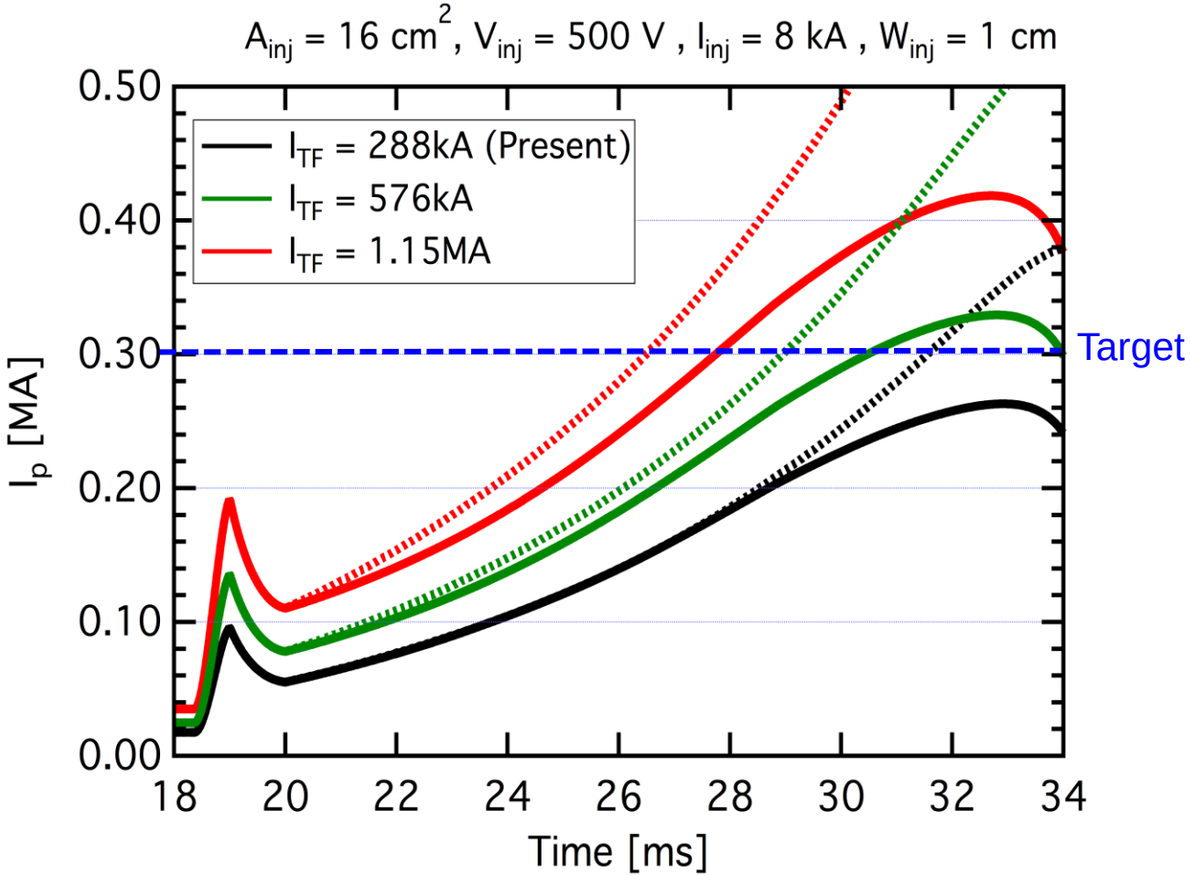
- New divertor coil array in upper & lower divertor regions
  - X-point control at 0.3 MA
- Added PF to improve shape & position control
- Initially, coil control will be pre-programmed
- Future control may include active feedback
  - Position control
  - Shape control



Increased Toroidal Field is Critical to the Non-Solenoidal Start-Up Mission

- B_{TF} increasing from 0.15 to 0.6 T
- Supports general start-up research:
  - Determining the scalability of LHI
  - Co-axial helicity injection (CHI)
  - Electron Bernstein Wave (EBW) current drive
- Requires doubling of TF power supplies & control channels
  - Number of H-Bridges from 6 to 12
  - Splitter/Combiner control from 12 to 24
- FPGA simplifies controls expansion

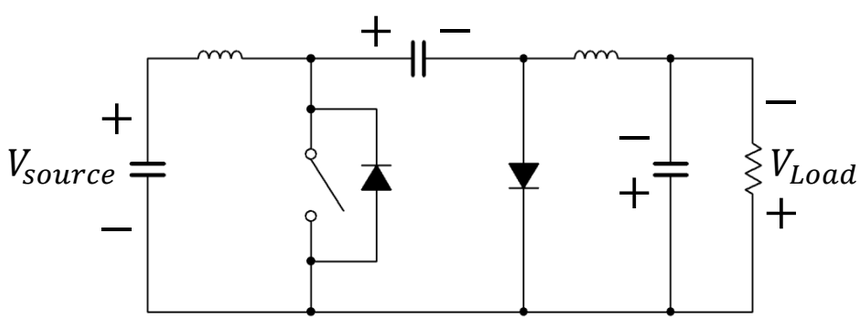
Projected Toroidal Field Scaling of I_P



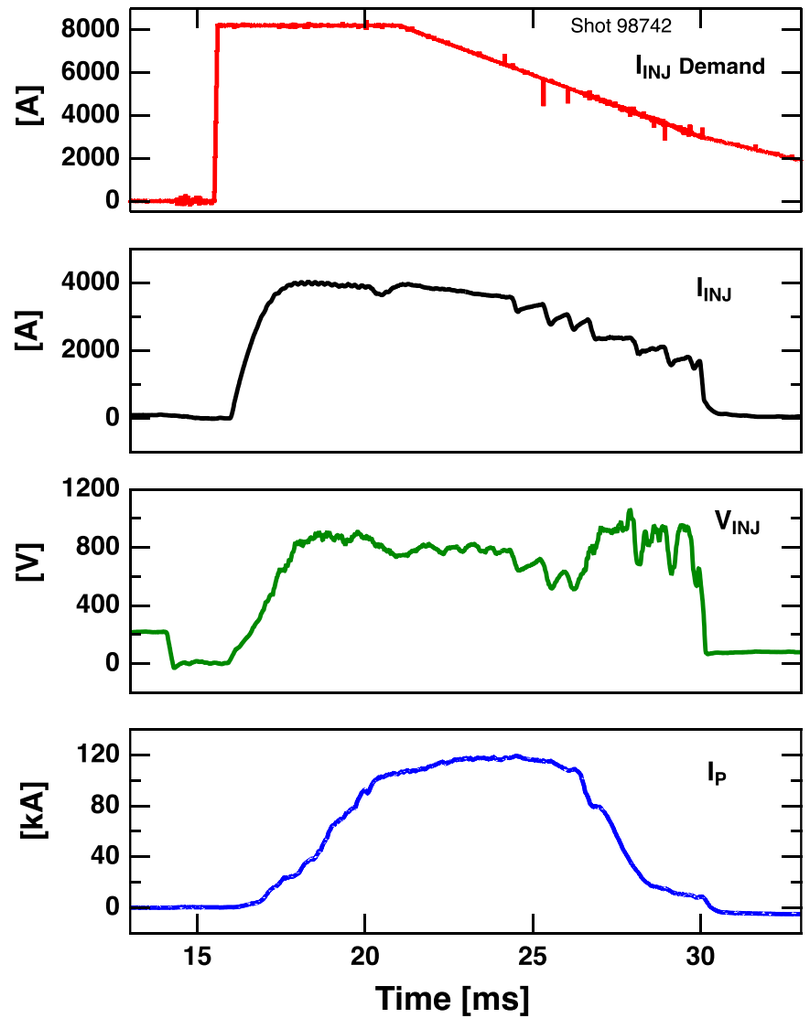
Injector Power Supply Topology Change Required for Low Ripple, Programmable $V_{inj}(t)$ Control

- H-Bridge regulation of injectors results in oscillations detrimental to the plasma
  - Typically operate with no active regulation
  - V_{inj} controlled with capacitor bank charge voltage
  - V_{inj} voltage droops during shot
- Ćuk power supplies produce a low ripple output with voltage gain capability
  - Low ripple → *active V_{inj} regulation during shot*
  - Voltage gain → *voltage droop compensation*
  - Voltage gain → *improved energy storage utilization*

Ćuk Converter Topology ⇨



Example of Regulation Induced Oscillations

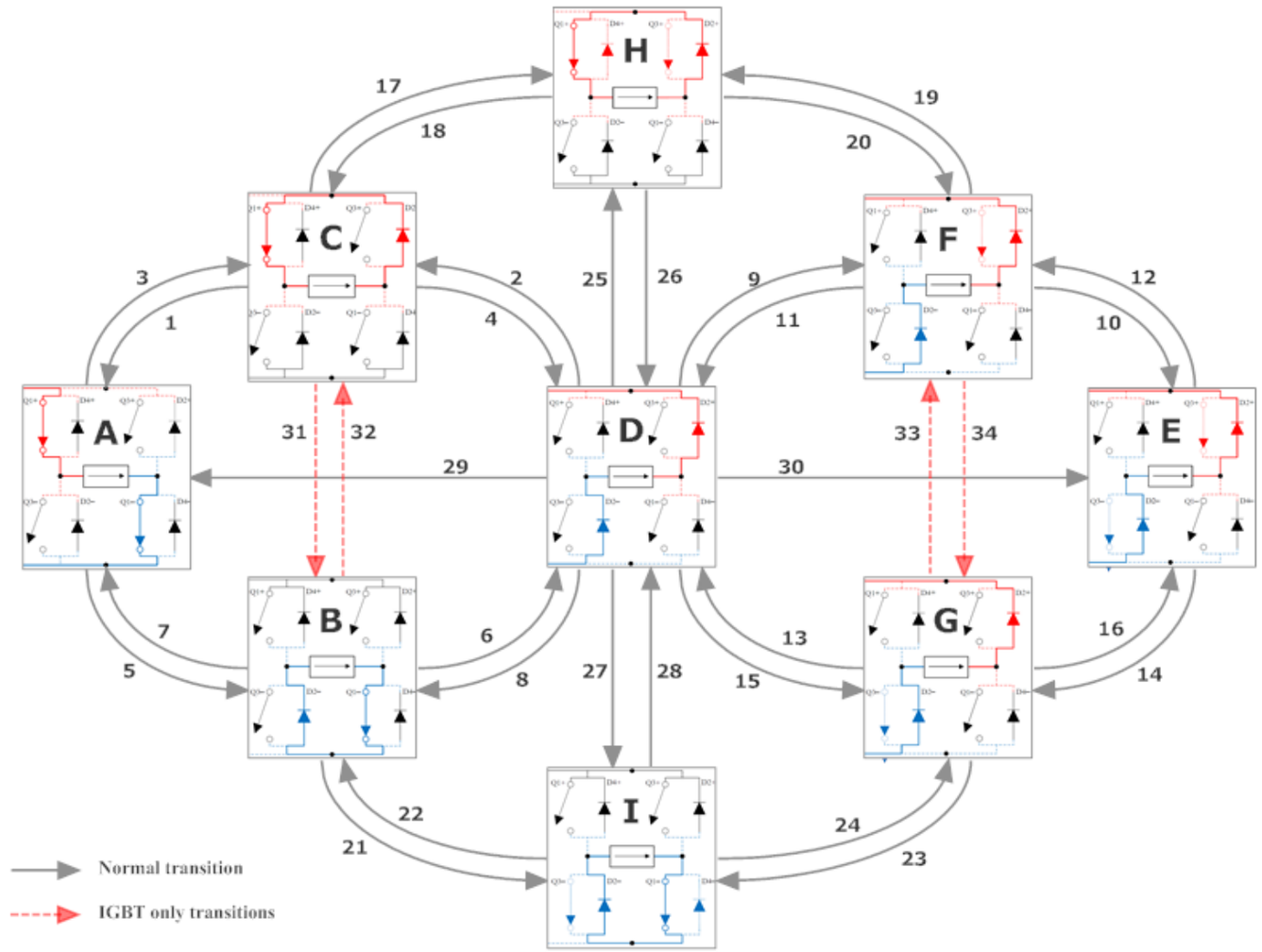


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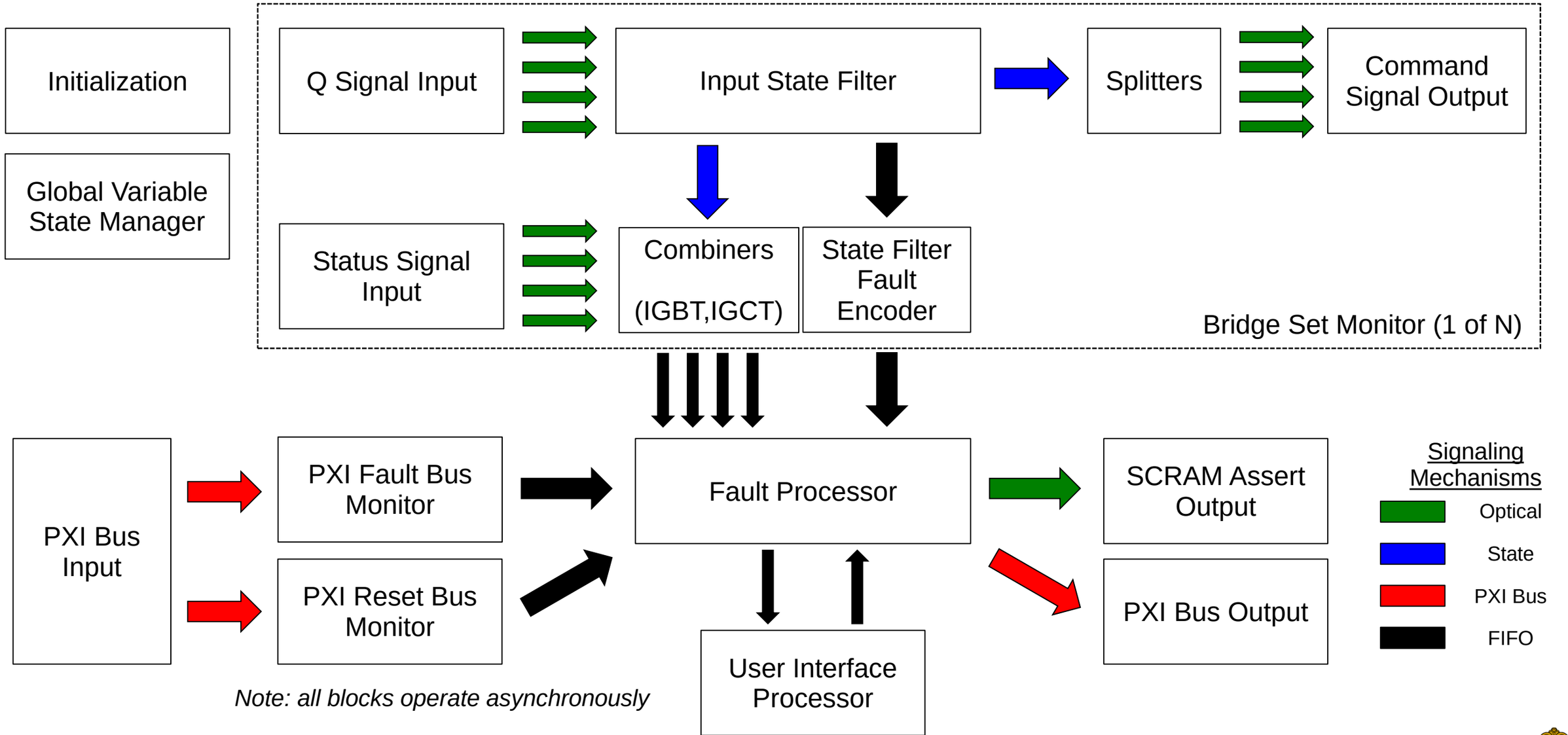
FPGA S/C Improves Device-Level Protections

- Splitter Functionality Retained:
  - Multiplexing of command signals to N bridges
- Combiner Functionality Retained:
  - Device-level interpretation of IGBT/IGCT status signals
  - Aggregation of bridge status signals to single assertion of "Coil Set OK"
  - Fault assertion for SCRAM system
  - Identification of faulted device
- FPGA Enabled Improvements:
  - Continuous monitoring of device status
  - State filtering for invalid PWM commands
  - Improved fault response time (25-200 ns)
  - Improved device protections

State-Diagram of Allowed H-Bridge States & Transitions



FPGA S/C Implementation Leverages Inherent Parallelism of LabVIEW & FPGAs for Asynchronous Operation



Note: all blocks operate asynchronously

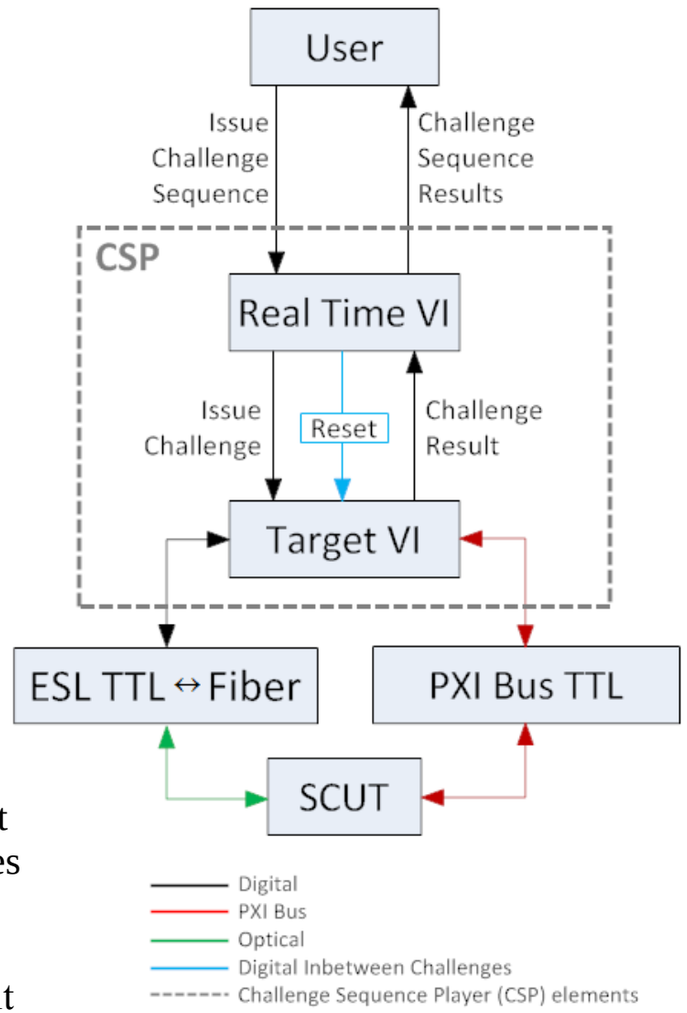
FPGA S/C Functionality Verified with Custom Testing Platform Prior to Deployment

- Test platform sourced arbitrary optical command signals to challenge the logic of the S/C Under Test (SCUT)
- Required 33 unique challenges
- Challenge results and fault response times reported to User
- Verified all S/C fault responses:
  - IGBT & IGCT status faults
  - Invalid state encoding
  - Invalid state transition command
  - Insufficient state dwell time

  } Fault Modes

  → No fault

Test Platform



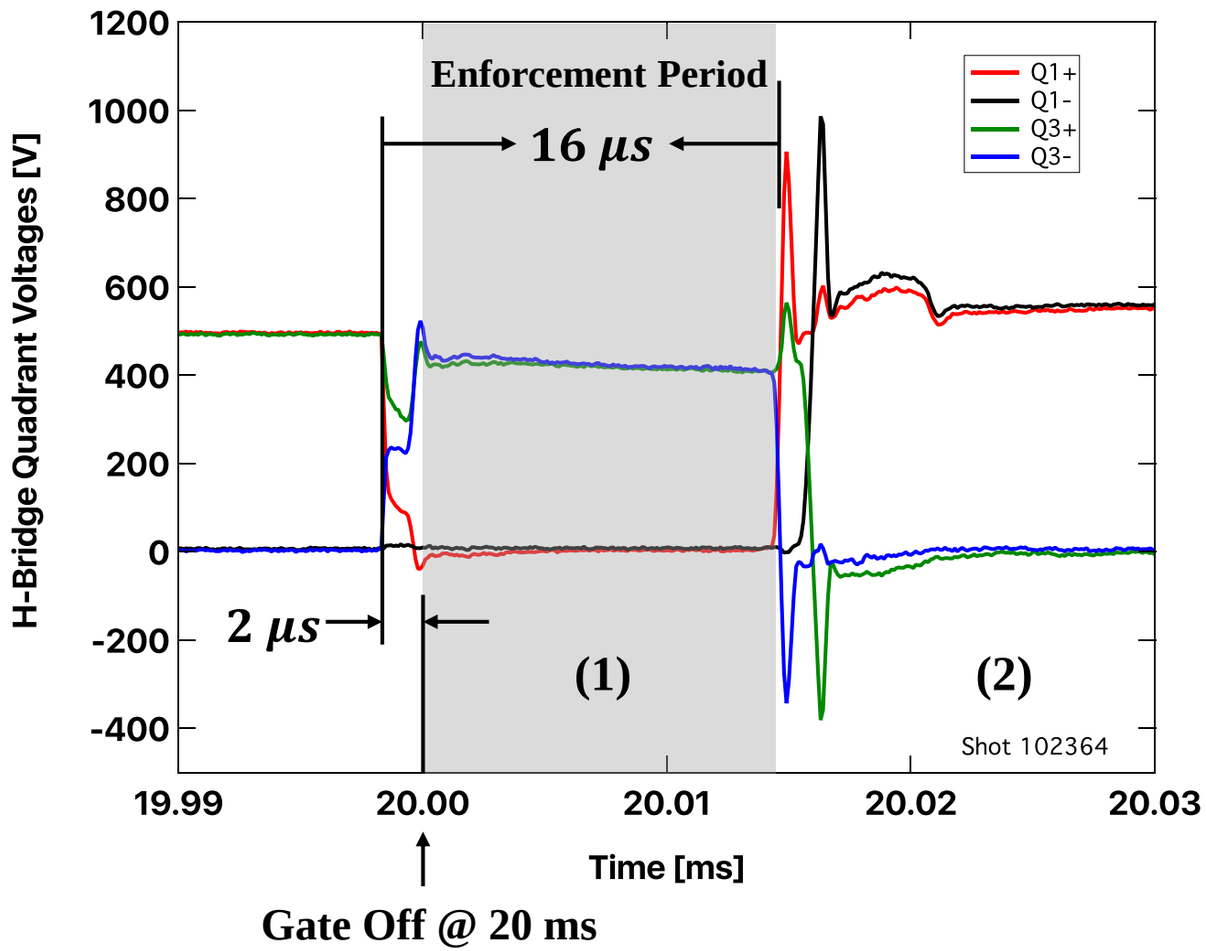
Present Power Supply Configuration

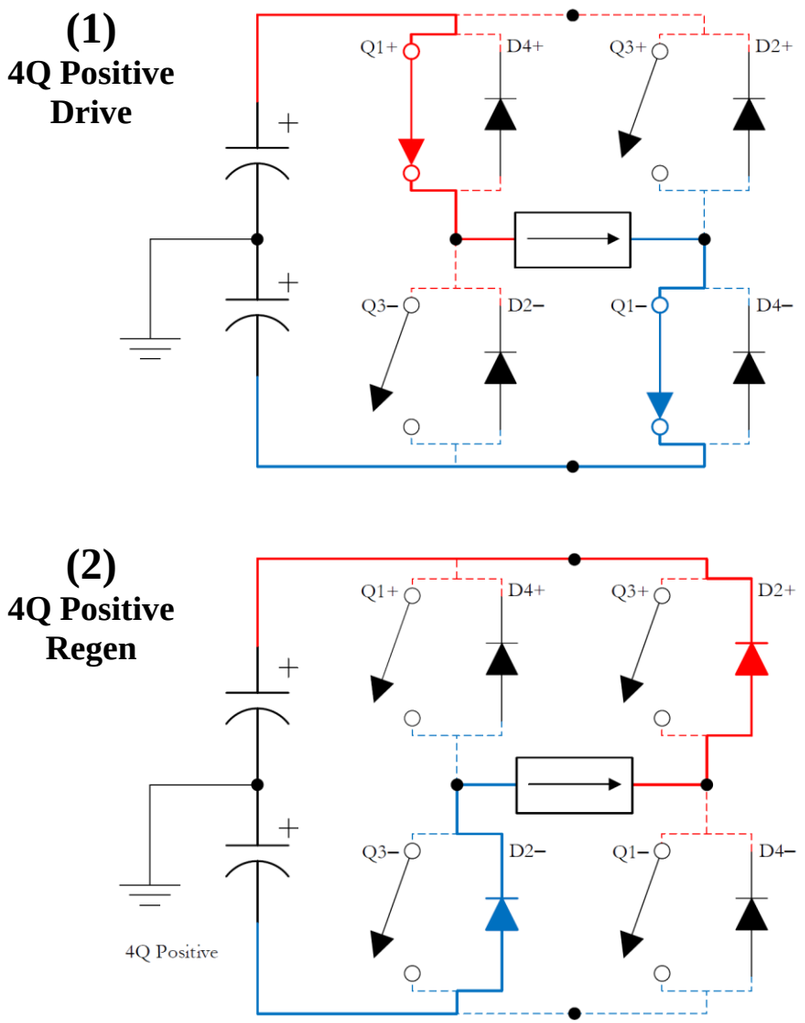
(FPGA S/C Deployed)

Load	Typ. V	I_{max} [kA]	# of Bridges	Bridge Type	S [MVA]
TF	900	24	6	2Q	21.6
PF 23	900	16	4	2Q	14.4
PF 67	900	16	4	2Q	14.4
PF 45	900	8	2	4Q	7.2
Radial Coil	900	4	1	2Q	3.6
Divertor Coil	900	4	1	2Q	3.6
Ohmic Solenoid	2200	32	8	4Q	70.4
Injector Arc	900	4	1	4Q	3.6
Injector Bias	2200	12	3	1Q	26.4

FPGA SC Deployment Increases Device-Level Protections; e.g. Minimum Dwell Time Enforcement

Example of Increased Protections and Circuit Schematics of H-Bridge States





Pulse Width Modulation (PWM) is a Voltage Control Technique Commonly Deployed In Power Systems

- Ratio of device (switch) On-time to Off-time known as the Duty cycle
- The output voltage is related to the input voltage through the duty cycle (D):

H-Bridge

$$V_{out} = D * V_{in}$$

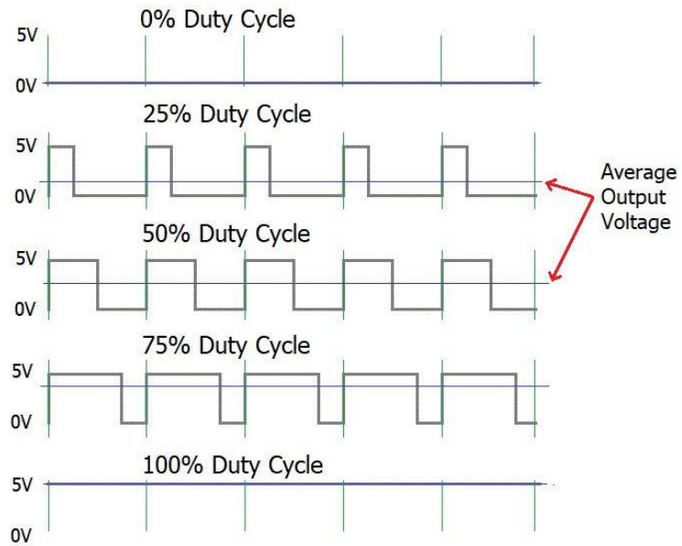
Ćuk

$$V_{out} = -\frac{D}{1-D} * V_{in}$$

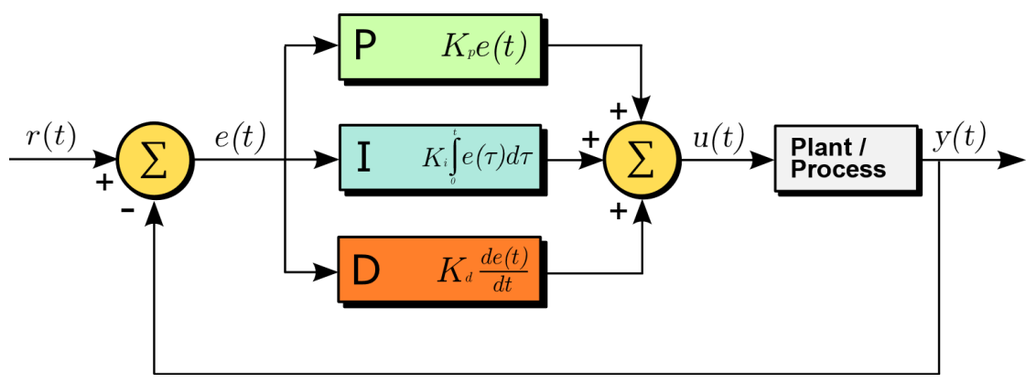
- Modulating the pulse width or duty cycle provides a means to control the output voltage
- FPGA controller will use PWM where the duty cycle or plant variable, $u(t)$, is generated by a Proportional-Integral-Differential (PID) controller:

$$u(t) = K_P e(t) + K_I \int_0^t e(\tau)d\tau + K_D \frac{de(t)}{dt}$$

Example of 5 V H-Bridge PWM



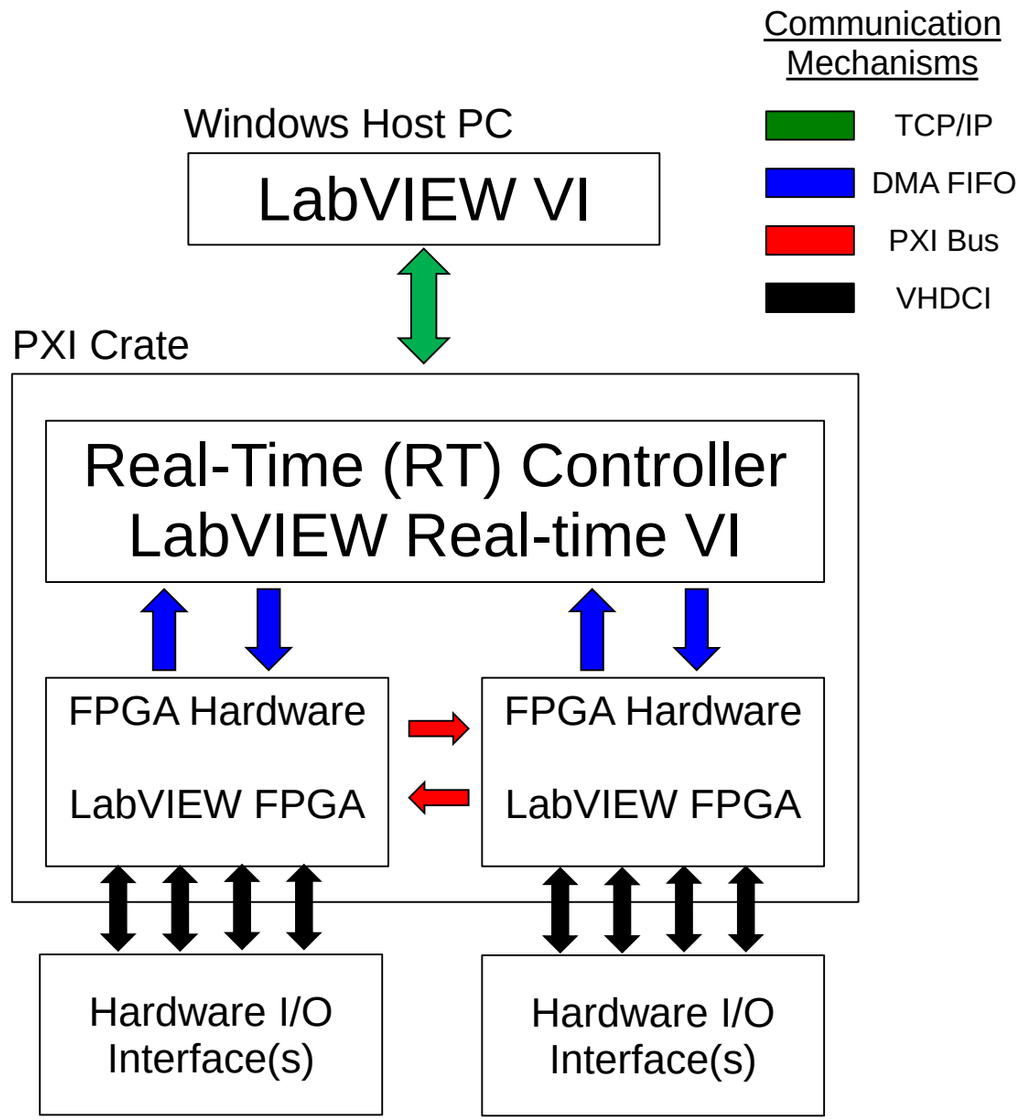
Aswinth Raj, https://circuitdigest.com/tutorial/what-is-pwm-pulse-width-modulation



A. Urquizo, http://commons.wikimedia.org/wiki/File:PID.svg

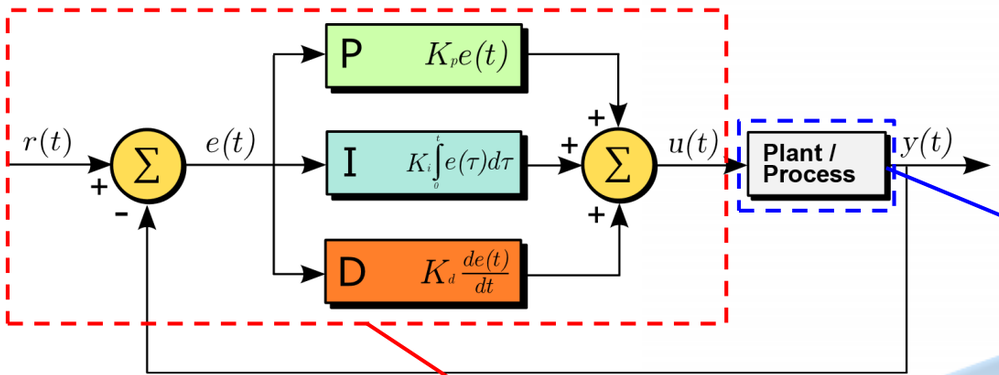
FPGA PWM Will Use a Multitiered Architecture: Windows Host ↔ RT Host ↔ Target

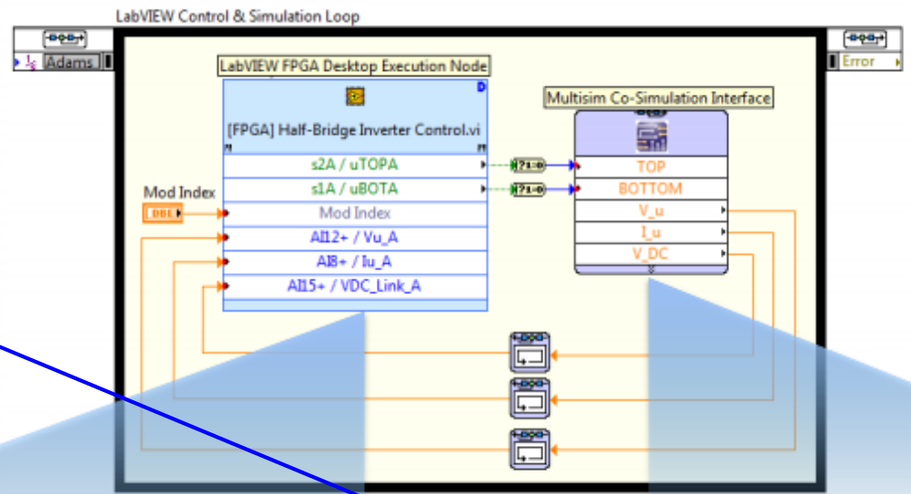
- Windows Host:
  - User interface (PWM settings, system status, etc.)
  - Main Control Code interface
- RT Host:
  - Between shots:
    - Update PWM settings from Windows Host
    - Write shot data to main data server
  - During shot:
    - Receive feedback signal, $y(t)$, and generate demand signal $r(t)$
    - Calculate error signal $e(t) = r(t) - y(t)$
    - Calculate plant signal, $u(t)$, from $e(t)$
    - Transmit plant signal to Target
- FPGA Target:
  - Measure feedback signal, $y(t)$ & transmit to RT
  - Receive plant signal, $u(t)$, from RT (signed duty cycle)
  - Use plant signal to decide on next action
    - State & duration of next PWM cycle

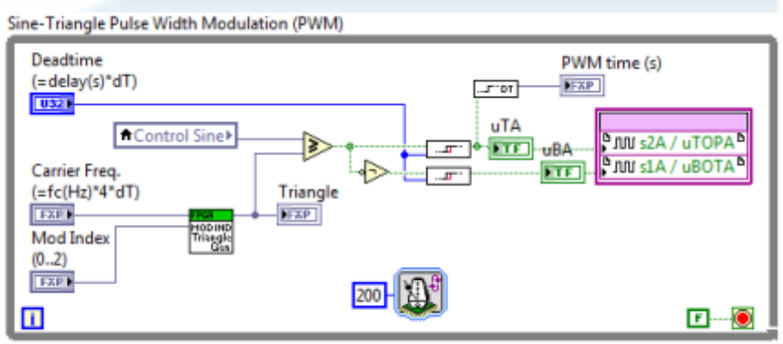


FPGA PWM Control Logic to be Verified with Coupled Simulation of LabVIEW FPGA Controller VI and Multisim Circuit Model

- LabVIEW simulation of PWM control signal (plant signal) generation
- Multisim simulation of circuit response (plant response) to control signals
- Data passed between simulation environments each time step

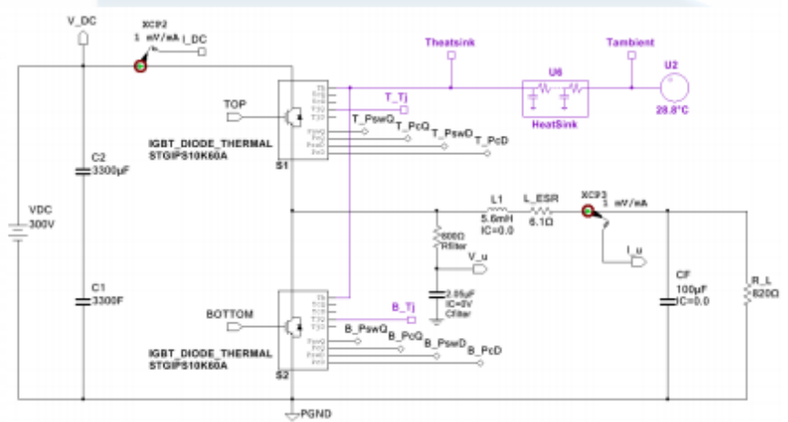






$u(t)$

$y(t)$

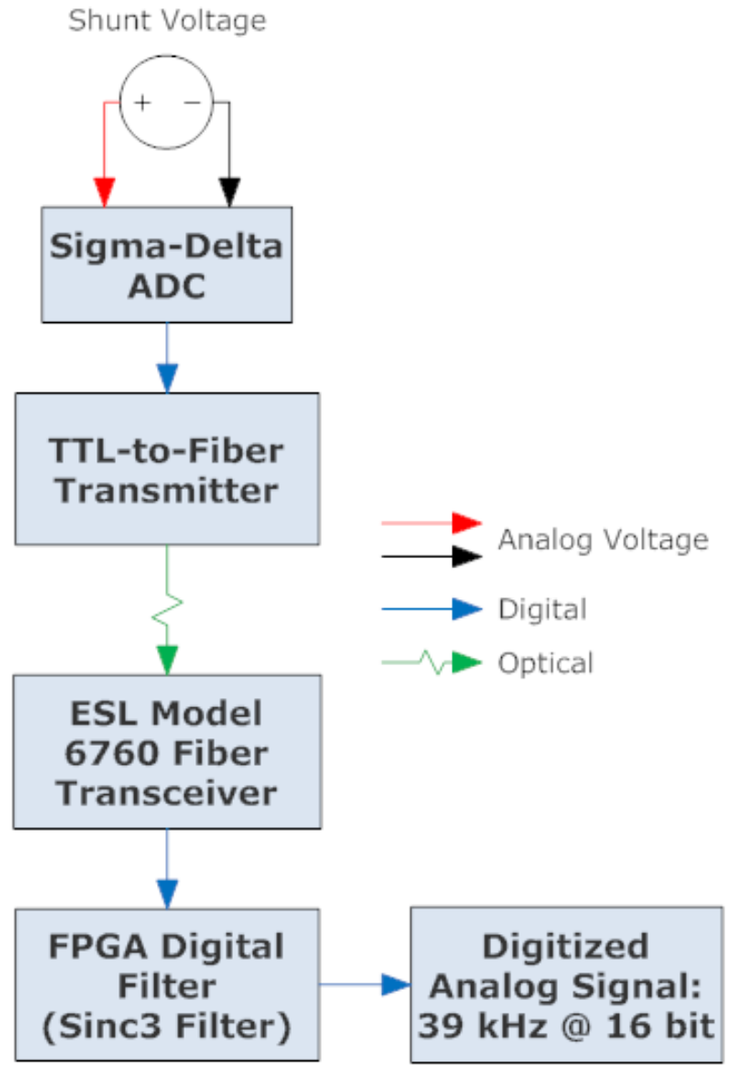


B. MacCleery, https://www.energy.gov/sites/prod/files/2016/11/f34/Panel%202_NI_MacCleery.pdf

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Optically Transmitted Local Shunt Voltage Measurement in Development for FPGA PWM Feedback Signal

- Current measured with series shunt resistor: $I = \frac{V}{R}$
- Shunt voltage locally converted to 1 bit stream with Sigma-Delta ADC
  - Voltage encoded in the duty cycle of the bit stream
- Bit stream transmitted ***optically*** to FPGA
- FPGA filters bitstream to recover analog signal
- Benefits include:
  - Linear response
  - Ability to measure DC current
  - Improved signal to noise ratio
  - No integration required

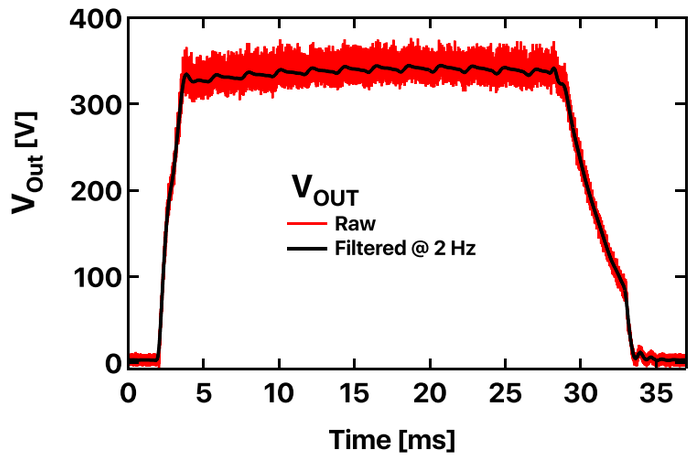


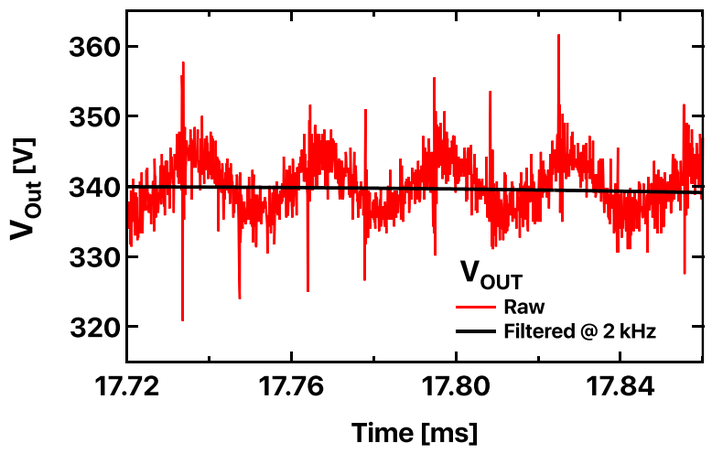
Single Ćuk Module Achieved ~25 ms Flat-Top at ~1.2 MW While Utilizing 60% of the Stored Energy*

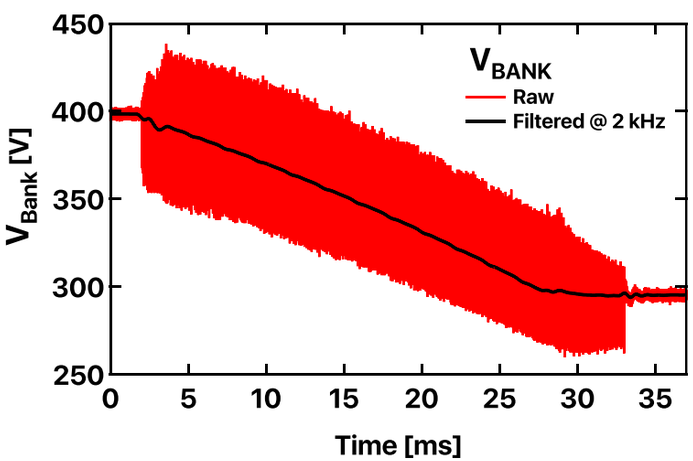
- Goal for future injector power supply is a low ripple Ćuk module at 400V & 4kA

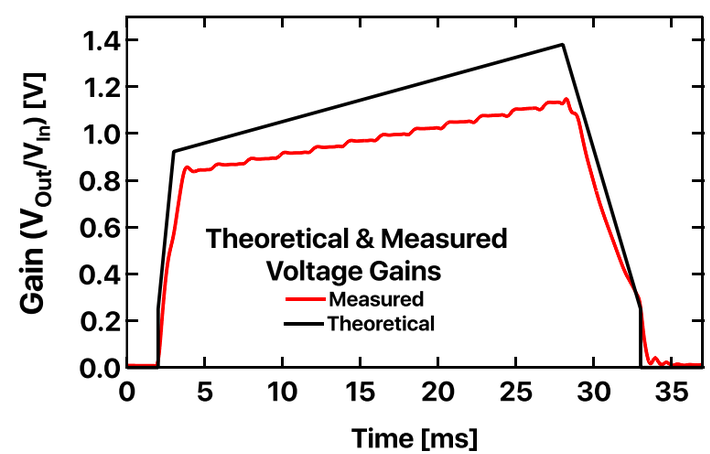
- Test results of an Eagle Harbor Technologies Ćuk module:
  - 340 V, 3.4 kA into 100 mΩ load
  - 60% stored energy used (40% to load)
  - No droop in V_{out} with 100 V droop in V_{bank}
  - 3% peak-to-peak ripple
  - Low frequency ripple can be designed away

Results of Ćuk Power Supply Prototype Testing





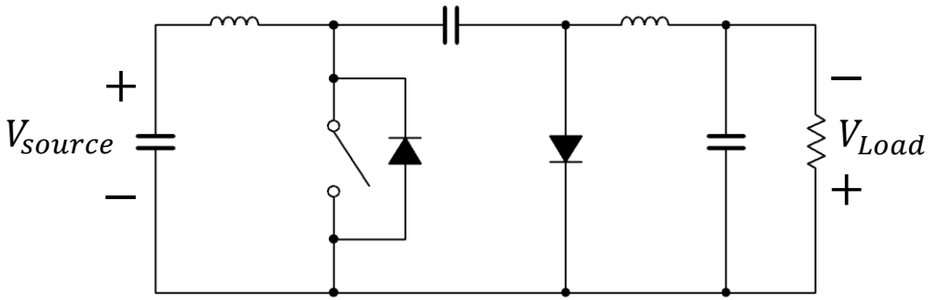




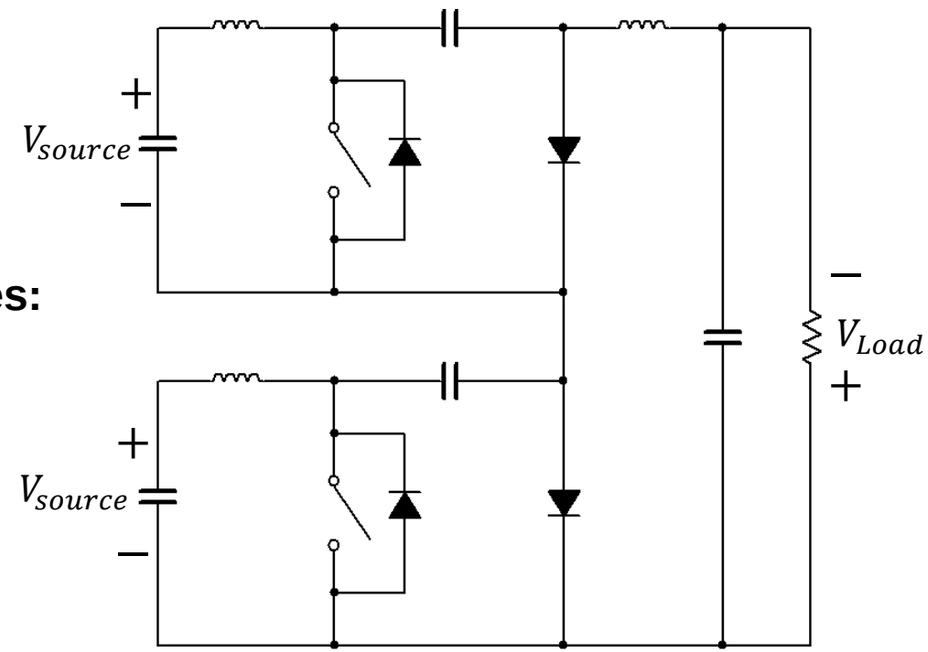
*In collaboration with A. Henson, Eagle Harbor Technologies, TP11.00126

Modular Ćuk Power Supply Design Enables Parallel & Series Topologies for Varying Voltages & Currents

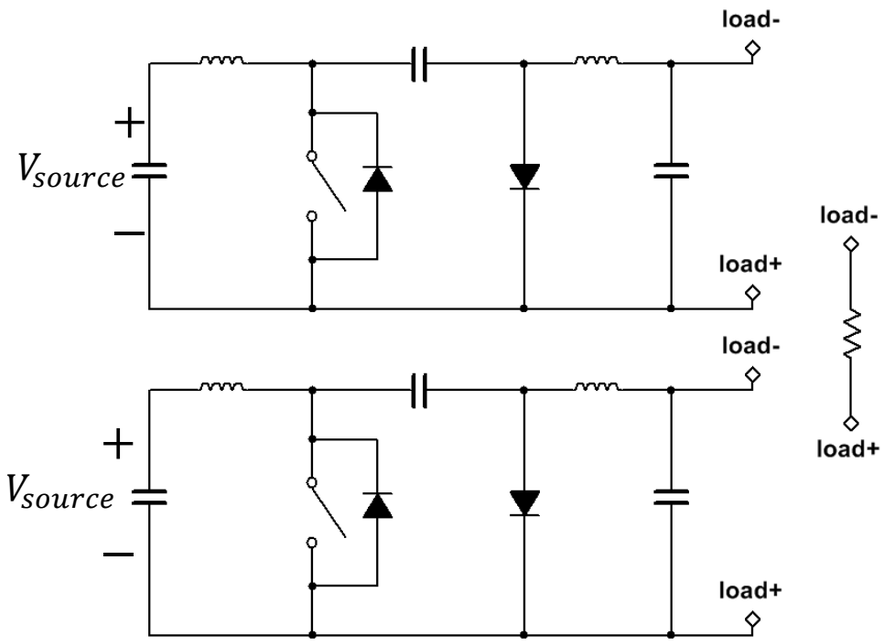
Single Module:
400 V & 4 kA



Two Series Modules:
800 V & 4 kA



Two Parallel Modules:
400 V & 8 kA



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Development & Deployment Plan for Power Supply & Control System Upgrades

Near-Term

- Complete FPGA SC deployment
  - Improves device protections
  - Enables OH experiments
- FPGA digital PWM
  - Programmable coil & LHI control
  - Advanced control algorithms
    - Combined feedforward & PID control
- DNB power supply & control
- Ćuk converter for injector Arc and Bias power supplies
  - Low ripple, programmable voltage control of helicity injection

Longer-Term

- Active control of helicity injection
- Active injector gas control for injector impedance control
- FPGA replacement of CAMAC timing modules
- RF/EBW power supply & control

Summary of Physics Studies and Experimental Improvements Enabled by Planned & Proposed Upgrades

- Improved device protections enable OH Experiments:
  - Impurity studies
  - Taylor limit studies
  - LHI to OH handoff
- $V_{INJ}(t)$ helicity injection control:
  - Improved helicity drive scans for model validation
  - Active control for improved $I_P(t)$ evolution
- Increased TF:
  - Exploration of higher TF operating space relevant to start-up on larger machines
  - Increased Taylor limit studies
  - CHI, EBW
- PF Expansion:
  - Improved divertor control
  - Improved shape & position control
  - Better coupling to helicity injectors
- DNB Control:
  - Plasma kinetic & impurity measurements
    - $\tilde{B}(R,t)$, $J(R,t)$, $T_i(R,t)$, $n_e(R,t)$, $n_Z(R,t)$
- RF/EBW Control:
  - Electron heating
  - Current drive

Overview of Pegasus Power Supplies & Control Systems

Physics Studies to be Enabled by Control Upgrades



Improved Device Protections from Initial FPGA SC Deployment



Progress Towards a Digital FPGA PWM Controller

Planned Upgrades to Control System & Power Supplies

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http://pegasus.ep.wisc.edu/Technical_Reports

